Single Chip GX/TGX Product Family Hardware Theory of Operation Manual

Sun Microsystems Computer Corporation
2550 Garcia Avenue
Mountain View, CA 94043
U.S.A.

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Preface

This manual describes the theory of operation of the single chip GX product family. The single chip GX product family currently consists of GX, GXplus, TurboGXplus, and TurboGX cards. The GX chip is also used on the CPU board of some machines such as SPARCstation IPX and SPARCstation LX. Most of the information covered in this manual is generic enough and applicable to any single chip GX product whether it is installed on an SBus card, or directly on the CPU board (e.g., SPARCstation IPX and LX). This manual will be updated, as necessary, to cover future products related to the single chip GX product family.

Note – This manual contains information on the TurboGX which is an unreleased product.

Audience for This Manual

This manual is for Sun internal use only by engineers, customer service technicians, and quality assurance engineers.

How this Book is Organized

Each chapter begins with an introduction that tells you what the chapter contains. By reading the introduction, you can quickly determine whether a particular topic relates to what you want to do. However, you should read at least chapter 1 to become familiar with the GX product family.

Summary of Contents

The contents of the chapters and structure of this manual are summarized below.

Preface describes the organization of this manual.

Chapter 1 contains an overview and the block diagram of the single chip GX card, a brief description of the key hardware elements, and a brief description of each sheet of the schematic diagram.

Chapter 2 describes the SBus Interface. It also describes the system configuration, SBus protocol design, signals descriptions, software model, and address maps.

Chapter 3 describes the SBus Interface block. It explains the SBus interface block functions, and various timing diagrams.

Chapter 4 describes the LSC core. It explains the LSC chip configuration diagram, LSC signal descriptions, testing methodology, and pinouts.

Chapter 5 describes the TGX core. It explains the TGX chip configuration diagram, TGX signal descriptions, testing methodology, and pinouts.

Chapter 6 describes the video memory and timing diagrams.

Chapter 7 describes in detail the Bt458 RAMDAC.

Chapter 8 describes in detail the Bt467 RAMDAC.

Chapter 9 describes the single chip GX cards configuration. In addition, it contains the specification summary, video timing diagrams, and video memory architecture of the GX, GXplus, TurboGXplus, and TurboGX cards.

Relevant Documents

Documents that contain information applicable to or which have been referred to in this document are listed below.

Part Number	**Description**
800-4453	*The Sun SBus Specification.* Describes the SBus from a Design Engineer's point of view.

800-5111	*GX Installation Guide.* Describes how to install the GX card into various Sun SPARCstations and SPARCsystems.
800-5940	*GXplus Installation Guide.* Describes how to install the GXplus card into Sun SPARCstation 2.
800-7579	*TurboGXplus Installation Guide.* Describes how to install the TurboGXplus card.
800-5112	*TurboGX Reference Card*. Describes address maps and register contents of the TEC and FBC sections of the TGX chip.
801-5339	*TurboGX/TurboGXplus Installation Guide*. Combines the installation instructions for the TurboGX and TurboGXplus cards.
	Computer Graphics: Principles and Practice by Addison-Wesley Publishing Co., ISBN-0-201-12110-7. Describes the fundamentals of computer graphics necessary to understand the design of the GX products.

Signal Levels and Signal Names

The following conventions are used with respect to signal names and levels:

Driven means that an output driver is sourcing or sinking current. Driven low means an output is driving the signal to 0V dc. Driven high means that an output is driving the signal to +5V dc.

Logical 1 (high) is the logical state of a signal driven to +5V dc. **Logical 0 (low**) is the state of a signal driven to 0V dc.

Asserted is the state of the signal used to initiate an action. **Unasserted** is the state of the signal used to terminate an action.

Both **active-high** and **active-low** signals are used. A signal name that is followed by an asterisk (for example, CSEL*) indicates that the signal is asserted active low (the logic 0 state). Conversely, a signal without an asterisk indicates that the signal is asserted active high (the logic 1 state).

Signals that are logically related are indicated by a common prefix followed by a number in angle brackets. For example, individual bits of the SBus data signals are labeled SBD<0>, SBD<1>, and so on. The entire 32-bit range of signals is labeled SBD<31.. 0>. (Note that the first number in the range indicates the most significant bit).

A timing diagram that shows a vector of signals driven both high and low at the same time normally indicates that each signal in the vector is stable and in its appropriate state. This condition may also indicate that the state of the signal is not significant during this period.

Off-page references are indicated by a five (or six) sided flag symbol containing the words IN, OUT, or BI, the page number, the horizontal coordinate, the vertical coordinate, and a direction symbol (> for input, < for output, and <> for bidirectional). For example, 4A5> refers to an input from page 4, sector A5, where A is the horizontal coordinate and 5 is the vertical coordinate.

Component Designators

Each component is assigned one of the following designators:

Designation	**Component**
C	Capacitor
D	Diode
J	Female Connector
L	Inductor
P	Male Connector
R	Resistor
U	Integrated circuit/resistor DIPs

The designator is followed by a number that distinguishes components of the same type.

Functional Description 1

This chapter provides functional description of the GX, GXplus,TurboGXplus, and TurboGX graphic accelerator cards. At Sun these cards are also known as LegoSC, Quadro Jr., and the TurboGX card (an unreleased product).

1.1 General Description

The GX, GXplus,TubrboGXplus, and TurboGX cards are SBus compatible 8-bit color/greyscale graphics accelerator cards. They are 100% software backward compatible with the LegoS4 and LegoP4. They can be used either with the old 66 MHz Sun color monitor or the new 76 MHz Sun color monitor.

The GX,TurboGXplus, and TurboGX cards are single-wide SBus cards that conform to the Sun single-wide Sbus card specification. The GXplus is a double-wide SBus card which conforms to the double-wide SBus card specifications. The output of these cards goes directly to the video monitor. Refer to *The SBus Specification* (Document Number 800-4453).

The GX, GXplus, TurboGXplus, and TurboGX cards are supported on many SPARCstations and SPARCsystems. Refer to Chapter 7 for details. Also refer to the *GX Installation Guide* (Part Number 800-5111), *GXplus Installation Guide* (Part Number 800-5940), *TurboGX/GXplus Installation Guide* (Part Number 801-5339) for GX configuration options.

1.2 Addressing Modes

The GX card contains a single frame buffer with a maximum resolution of 1152 x 900 pixels with 8-bits per pixel. It is used in one of three addressing modes:

- HRMONO. One plane, antialiased, high-resolution monochrome mode. The address space is enlarged by four times the actual screen resolution for both the x and y coordinates. The software therefore sees a frame size of 4608 x 3600 subpixels with 16 subpixels for each physical pixel. The GX card maps this large address space into the frame buffer address space resulting in a 5-bit greyscale value for each pixel. The greyscale values can be used to partly turn on selected pixels to fill in the jagged or sawtooth forms that can appear on diagonal lines. This technique of improving the look of a graphic image is called antialiasing.
- COLOR1. One plane color mode where monochrome data from the CPU is expanded to an eight plane frame buffer format by duplicating the result of the operations performed on the one plane source across all eight planes in the frame buffer. All pixels in the plane are displayed in either the background or foreground color. The addresses are pixel coordinates.
- COLOR8. Eight plane color mode where one byte in memory is mapped to one pixel of the display. This allows the display of 256 (2^8) colors out of a palette of 16, 777,216 (2^{24}) colors through the use of a lookup table (LUT). The addresses are pixel coordinates. This mode is the only mode used for dumb (unaccelerated) frame buffer access.

1.3 Graphics Commands

The GX products accelerate three basic graphics commands normally done in software:

- The DRAW command draws points, lines, triangles, rectangles, and quadrilaterals using integer coordinates. A 16 by 16 monochrome repeating pattern can be used when rendering an image with the DRAW command. The pattern can be aligned in both x and y. This pattern can be overridden by specifying an option for a pattern of all ones or zeros. An optional raster operation (RasterOp) may be done during the transfer. The RasterOp determines a new destination pixel value by applying a logical operation on the corresponding source and destination pixels. A linear RasterOp can also

be used for greyscale antialiasing. The RasterOp also expands the monochrome pattern data into the specified foreground and background colors.

- The BLIT (Block Image Transfer) command moves a rectangular block of pixels from one location (the source) to another equivalent-sized location (the destination) within the frame buffer. An optional RasterOp may be done during the transfer. The BLIT command always assumes COLOR8 mode and pixel coordinates.
- The FONT command allows a precomputed image using character bit maps to be transferred from the CPU into the frame buffer one image at a time. Images described in a single plane data structure can be written to the frame buffer in HRMONO and COLOR1 mode. Images described in an eight plane data structure can be written to and read from the frame buffer in COLOR8 mode. The data is transferred 32-bits at a time representing up to 32 monochrome pixels, 32 monochrome subpixels, or four 8-bit color pixels. An optional RasterOp may be done.

1.4 Graphics Operations

The graphic operations performed by the above commands take place within a clipping widow. The affect of the clipping window depends on GX modes: render mode or pick mode. In render mode, the card clips an object to the size of the clip window and then renders it into the frame buffer. In pick mode, if any part of the object is inside the clip window, it is considered picked and the pick status bit is set. This is used to indicate if a graphic operation would have written data to the frame buffer. The object is not rendered to the frame buffer in pick mode.

1.5 Raster Operations

Raster operations (RasterOps) allow boolean operations to be done in pixel mode (COLOR1 or COLOR8) and linear operation to be done in antialiasing mode (HRMODE). There are 16 different boolean operations (linear mode is a subset of these 16) that may be done on the source and destination pixels. Foreground and background colors may be specified to provide mapping from monochrome data to color data.

Two types of masking are used. A plane mask is used to enable writes for any of the 8 planes. A 32-bit pixel mask aligned to the screen is used to enable writes for individual pixels within a plane. This is called stenciling.

The card supports up to 4 by 4 matrix arithmetic to translate a two- or three-dimensional image from one location to another, to scale an image, and to rotate an image about an arbitrary point. The interface can read and write in these formats. These transformations can accept and produce signed integer, signed fixed point (16.16 bits), or single precision IEEE floating-point coordinate values.

The GX, GXplus, and TurboGX card hardware supports a generalized graphics transformation pipeline consisting of an optional MV (modeling and viewing) transform, an optional 2-D/3-D clip check, an optional perspective divide, and an optional VDC (virtual device coordinates) transform. The hardware also supports generalized vector operation allowing it to do matrix concatenations, dot products, or even convolutions.

Transformation results can be optionally loaded directly into the rendering engine (Frame Buffer Controller) for display.

The cards provide a 32 by 32 pixel hardware cursor in three colors. The cards also provide programmable vertical and horizontal timing signals for the monitor. The cards use a single ASIC (Application Specific Integrated Circuit) to provide a high degree of functionality on a small card.

A block diagram of the Single Chip GX graphics accelerator card is shown in Figure 1-1.

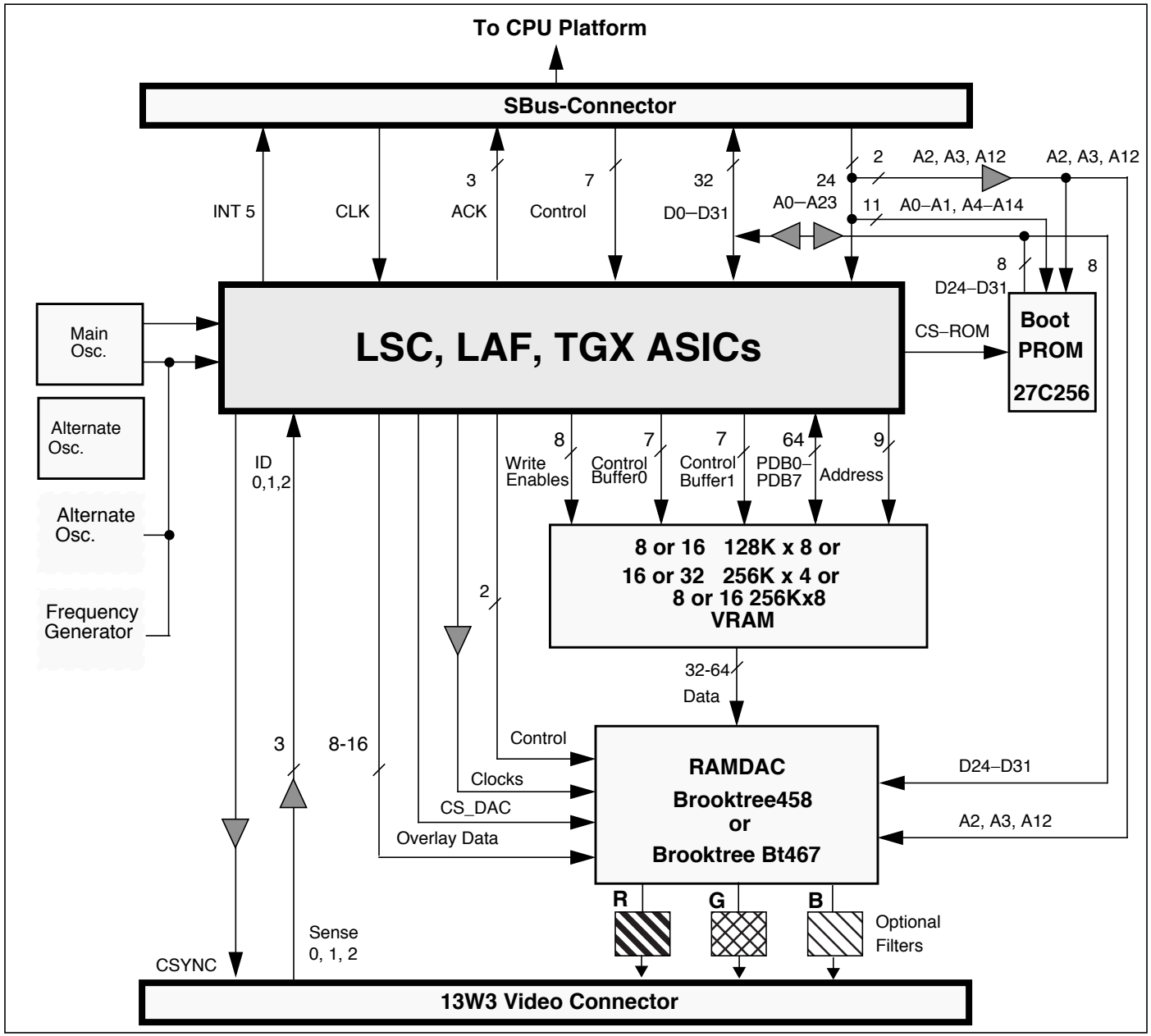


Figure 1-1 Single Chip GX Generic Block Diagram

1.6 Key Hardware Features

The key hardware elements shown in Figure 1-1 are described in the following text.

1.7 SBus Connector

The GX, TurboGX, and TurboGXplus cards connects to the SBus on a Sun CPU board through a 96-pin male mini-DIN connector. This connector, J1, is used for both signal and power. The GXplus, which is a double-wide card, uses two of these connectors on the CPU board: J1 and J2. The J1 connector is used for both signal and power, and J2 connector is used for power only. The LSC chip accepts commands and data through the 32-bit SBus data path and puts out the appropriate pixel information on the 64-bit pixel data path.

Table 1-1 shows the 82 signals and 14 power and ground connections for the SBus. The I/O column is from the GX card's perspective. Refer to Chapter 2, "SBus Interface" for J1 pinout information. Using the same power connections on both connectors allows for a greater current capacity

Table 1-1 SBus Signal Summary

Name	I/O	Description	Driven By
SBPA<23. 0>	I	Physical Address	Controller
SBSEL*	I	Slave Select (1 per slave)	Controller
SBD<31.. 0>	I/O	Data	Master and GX chip
SBSIZ<2.. 0>	I	Transfer Size	Master
SBRD	I	Transfer Direction	Master
SBCLK	I	SBus Clock	Controller
SBAS*	I	Address Strobe	Controller
SBACK (2..0)*	O	Transfer acknowledgment	GX and Controller
SBRESET*	I	Reset	Controller
SBIRQ5*	O	Video interrupt Request (open drain)	GX chip
Ground (7 pins)	-	Ground	Controller

Table 1-1 SBus Signal Summary

Name	I/O	Description	Driven By
+5V (5 pins)	-	Power (2A per slot)	Controller
+12V (one pin)	-	30mA	
-12V (one pin)	-	30mA	

1.7.1 Boot PROMs

The GX card contains an FCode (Forth) program that:

- Provides basic functionality
- Uniquely identifies the card

Contains auto-configuration information, preforms boot time initialization for the card, passes additional configuration information to the operating system, etc. The boot PROM contains the following information starting at physical address 0:

- A one-byte magic token; the constant 0xFD
- A one-byte version number of the GX card
- A two-byte check sum computed over the whole program
- A four-byte length that includes the length of the header and the end token; this is equal to the offset to the first byte that is not part of the program.
- Zero or more program bytes of FCode; this must be a properly constructed Forth program.
- A one-byte end token; the constant 0x00.

1.7.2 Video Memory

Depending on the card configuration, the VRAM section consists of a bank of 128K x 8, 256K x 4, or 256K x 8 VRAM chips. This provides a single frame buffer of medium resolution (1152 × 900 with 8-bits of color per pixel). The video memory is located on the component side as well as the solder side of the TurboGX card.

For the memory, the LSC provides the RAS and CAS strobes along with the appropriate addresses to the VRAMs. The pixel write strobes are also generated out of the LSC chip directly into the VRAMs for the GX card, and via external OR gates for the GXplus card. The VRAM is accessed through a full 64 bit data path from the LSC. The shift clock lines are split for loading into SCK0 and SCK1. The RAS and CAS strobes along with the addresses and the pixel write enables are provided by the LSC chip. The video (serial) outputs of the VRAMS can be multiplexed by four or eight (software selectable) to provide the appropriate input for the RAMDAC used.

1.7.3 RAMDACs

Depending on the card configuration, either Bt458 or Bt467 RAMDAC is used. The RAMDAC consists of some pixel data registers, and a 256 x 24 color lookup table with triple 8-bit video D/A converters. Each pixel value from the video memory is used to look up the proper values to drive the red, green, and blue video monitor guns. The video outputs generate RS–343A compatible Red, Green, and Blue video signals which are set up to drive doubly-terminated 75-ohm coax cable. The reference voltage is generated by an LM 385 device. The EMI low pass filters may be used on the Red, Green, and Blue video outputs. The sense information (designating monitor type) is fed back to the LSC through a buffer and the composite SYNC is buffered to the monitor as well.

1.7.4 LSC/LAF/TGX

The LSC (LSC/LAF/TGX) is the main component of the Single Chip GX based cards. The graphic operations accelerated by the GX card are divided between the two major blocks of the LSC: FBC and TEC.

The FBC portion of the LSC chip executes the DRAW, BLIT, and FONT commands. It clips an image to the viewing window and allows an object to be picked. It also controls various attributes: foreground and background color, RasterOps, plane mask, pixel mask, and the pattern used for the operation. It is also responsible for all VRAM address multiplexing.

The TEC portion of the LSC chip transforms an image from world coordinates to viewing coordinates. It clip checks the image against a unit perspective viewing pyramid; performs a perspective divide; and transforms the image into virtual device coordinates and then into screen coordinates. The results of

the TEC transform can be automatically loaded into the FBC over the local buses. The TEC block also provides a programmable hardware cursor and programmable timing for the monitor and VRAM control functions.

The LSC is a large size ASIC which also (in addition to TEC/FBC functionality) handles the SBus interface (control, address, and data), VRAM interface, (control, address, and data), and the RAMDAC interface (overlay, data, clock, and control).

1.7.5 *Video Output Circuitry*

The information between the monitor and the frame buffer is passed through the video cable connecting them. The current Sun video cable contains three mini-coaxes as well as five twisted pairs. Table 1-2 shows the current video output pin assignments.

The video output connector P1 is a 13-pin D-connector with three coax pins for the red, green, and blue gun signals. The pinout for the video output connector is shown in Table 1-2.

Table 1-2 Video Output Connector Pin-Out

Pin	Function	Sun Usage
A1	Red	Coaxial receptacle 75 Ohm
A2	Green	Coaxial receptacle 75 Ohm (grayscale video)
A3	Blue	Coaxial receptacle 75 Ohm
2	Reserved	N/C
6	Reserved	N/C
5	CSYNC	Combined H/V Sync
3	S2	See Table C-3
8	S1	See Table C-3
9	S0	See Table C-3
4	GND *	Pin reference to frame buffer ground only
1	Reserved	N/C
7	Reserved	N/C
0	Cgnd	Return for pin 5

Sreturn = Logic ground, Pin 4
N/C = Not Connected

Table 1-3 Sense Pin Allocation

Code	Scan Rate	Pin 3 Sense 2	Pin 8 Sense 1	Pin 9 Sense 0
7 No Monitor	1152 x 900 66 Hz	N/C	N/C	N/C
6	1152 x 900 76 Hz	N/C	N/C	GND *
5	1024 x 768 60 Hz	N/C	GND *	N/C
4	1152 x 900 76 Hz	N/C	GND *	GND *
3	1152 x 900 66 Hz	GND *	N/C	N/C
2	1280 x 1024 76Hz	GND *	N/C	GND *
1	1600 x 1280 76Hz	GND *	GND *	N/C
0	1024 x 768 77 Hz	GND *	GND *	GND *

N/C = Not Connected (logical high through pullup resistor)
Sreturn = Logic ground, Pin 4 (logical low)

Note – Depending on product specific requirements, conformance with the above table may be waived.

1.8 What the Schematics Contain

The contents of each sheet of the schematics are described below. Please note, the schematics are not included in this manual.

GX Card (LegoSC) Schematic (Part Number 502-1672)

Sheet 1 contains the bus interface/frame buffer control.

Sheet 2 contains the video memory.

Sheet 3 contains the video/monitor control.

Sheet 4 contains the SBus interface.

GXplus (Quadro Jr.) Schematic (Part Number 502-1717)

Sheet 1 contains the bus interface/frame buffer control.

Sheet 2 contains memory buffers.

Sheet 3 contains write buffers.

Sheets 4 and 5 contain bank 0 video memory.

Sheets 6 and 7 contain bank 1 video memory.

Sheet 8 contains video/monitor control.

Sheet 9 contains SBus interface.

Sheet 10 contains various decoupling capacitors for the LSC, VRAM, and SBus oscillator. Also included are generic decoupling capacitors.

TurboGX Schematic (Part Number 502-2038)

Sheet 1 contains the bus interface/frame buffer control.

Sheet 2 contains write buffers.

Sheet 3 contains bank 0 and 1 memory.

Sheet 4 contains video/monitor control.

Sheet 5 contains clocks.

Sheet 6 contains information on the SBus connector, decoupling capacitors for the TGX, VRAM, and SBus oscillator.

TurboGXplus Schematic (Part Number 502-2253)

Sheet 1 contains the bus interface/frame buffer control

Sheet 2 contains write buffers

Sheet 3 contains bank 0 and 1 memory

Sheet 4 contains video/monitor controls

Sheet 5 contains information on the SBus connector, decoupling capacitors for the TGX, VRAM, and SBus oscillator.

SBus Interface 2

This Chapter provides the functional description of the SBus interface to the Single Chip GX, GXplus, TurboGXplus, and TurboGX card.

Note – The SBus interface to the GX card mentioned in this chapter also applies to GXplus, TurboGXplus, and TurboGX cards.

2.1 SBus Description

The SBus is a high performance 32-bit bus that allows the addition of small add-in cards to highly integrated desktop computers. The SBus design is for use as a motherboard bus, not as a backplane bus. It is a chip-level bus which is intended for chip-level interconnections between components in microprocessor-based systems. The design is optimized for use with CMOS and surface mount components.

For a complete description of the SBus from a Design Engineers point of view, Refer to *The Sun SBus Specification* (800-4453).

The principle features of the SBus used in the Single Chip GX card design are

- 32-bit data path
- Uses 24-bits of the available 28-bit physical address
- Design operates synchronously to allow operation over the full range of SBus clock rates (16.7 to 25 MHz)

- Uses one of the seven shared interrupt levels
- Uses data transfer sizes of 1, 2, and 4 bytes from the allowable 1, 2, 4, 8, 16, 32, and 64 byte transfer sizes (burst mode not supported)
- Automatic configuration of the card using machine independent code
- All signals are sampled on the rising edge of the clock
- Geographical Addressing where a slave select (SBSEL*) signal is used to select a particular slave thus eliminating the need for slave address jumpers
- Provides for Direct Virtual Memory Access (DVMA) by all bus masters, which greatly simplifies operating system and software memory management

2.2 *System Configuration*

The SBus configuration used with the GX card is a host-based system (see Figure 2-1). It uses a master-slave design consisting of three elements:

- **The SBus CPU master.** This is the Sun CPU on the motherboard. It uses the SBus as its principal I/O bus. The master selects a slave (for example, the GX card) using a virtual address. It then initiates a bus cycle to transfer data to or from the slave. Note that the CPU master does not connect directly to the SBus; it connects to an SBus controller, which connects to the SBus.
- **The SBus controller.** The controller provides a special path that the CPU uses to gain access to the bus. It also translates the virtual address that the master places on the data lines into a physical address that it places on the address lines. The controller issues a slave select signal (SBSEL*) appropriate to the translation of the virtual address. It then starts an SBus cycle by asserting address strobe (SBAS*). The controller is not a physically distinct object; it is part of the CPU motherboard.
- **The SBus slave.** This is the element that adds additional functionality to the system. It responds with an acknowledgment to a slave select and address strobe initiated by the master. Each SBus Expansion Slot has an independent slave selection line. This signal is named SBSEL* for the GX card. It is used to select the SBus slave that is active during the current cycle.

The master identifies a slave by issuing address `s4base` + 0, where `s4base` is the base address of the slot the card is installed in. Location 0 of each slave's address space contains a series of bytes that identify the card's manufacturer, model number, etc.

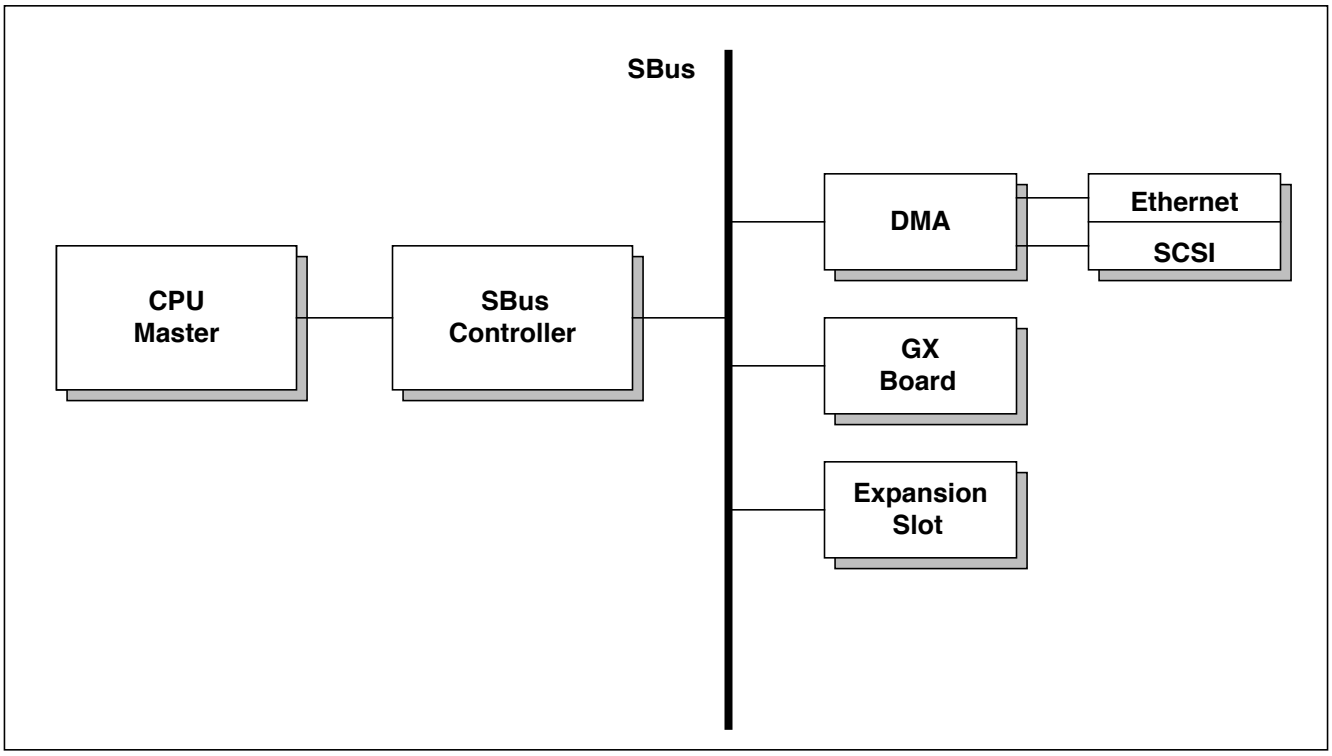


Figure 2-1 Host-Based SBus System

2.3 *Sbus Protocol Design*

The SBus protocol in systems using the Single Chip GX card is designed around three principles:

Synchronous Operation. The SBus controller generates a fixed-frequency clock between 16.7 and 25 MHz with a clock skew of 2.5 nS or less. This frequency is based on the CPU clock rate and is fixed for each system type. All signals are synchronized to the clock by sampling them on the rising edge of the SBCK

clock. These signals are driven so that they have a setup time of 15 nS and a hold time of 2.5 nS. The SBIRQ<5> interrupt signal is the only asynchronous signal.

Active Drive. Before a source removes its drive for an asserted tri-state control signal, the signal is actively driven to the unasserted state. This provides fast operation without the need for low-resistance pullup resistors and output drives capable of sinking the additional current through the pullups.

No Driver Overlap. Except for open-drain interrupt signal, no signal is driven by two outputs during the same clock cycle. Thus, output drivers never "fight", which can result in unreliable operation and excessive power dissipation.

2.4 SBus Cycle

The basic SBus cycle is shown in Figure 2-2. The cycle starts when the SBus controller places a memory address on the physical address lines (SBPA), asserts address strobe (SBAS*), and asserts a slave select (SBSEL*).

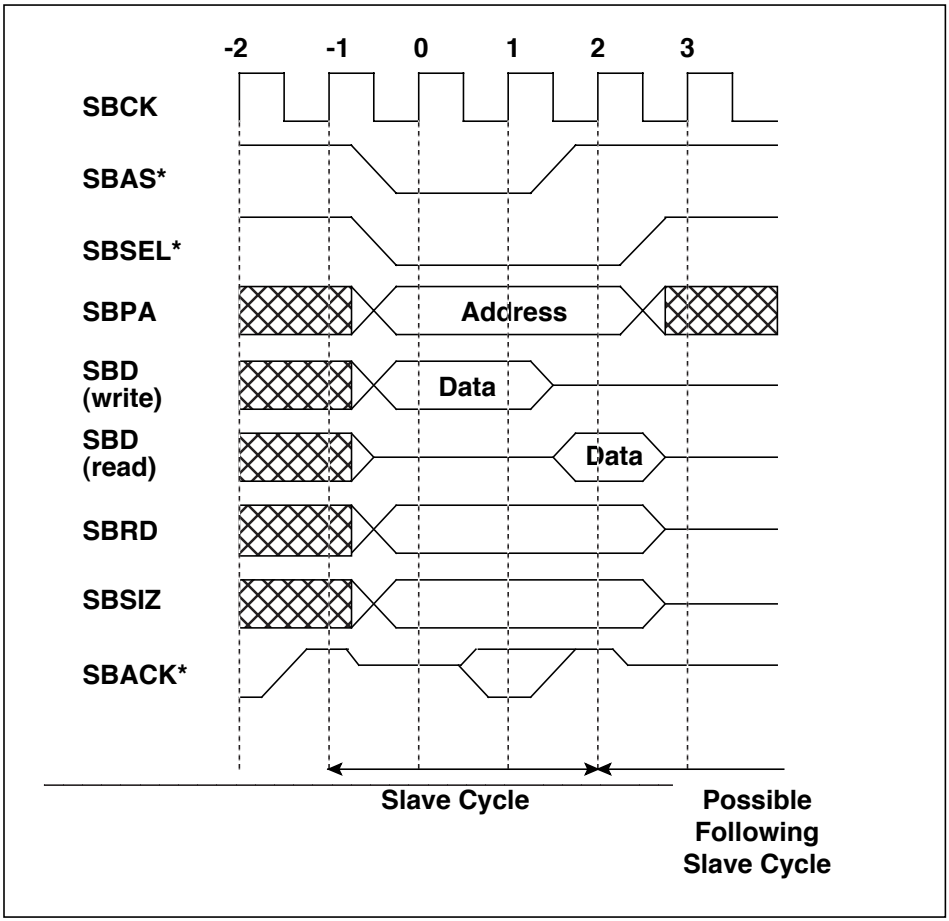


Figure 2-2 Basic SBus Cycle

For a write, the controller unasserts read (SBRD), asserts the transfer size SBSIZ<2..0>, and drives the data lines (SBD<31.. 0>). The slave has up to 255 clock cycles to perform the requested transfer and issue the proper acknowledgment SBACK<2..0>. For single word transfers, the slave drives the SBACK<2..0>, signals back to the idle (unasserted) state for one clock cycle, and then removes its drive in the following clock cycle.

The LSC does not use burst mode and will issue an error acknowledgment if attempted.

For a read, the acknowledgment is pipelined. That is, the slave generates the acknowledgment, and then drives the data lines on the following clock cycle for exactly one clock cycle.

2.5 Signal Descriptions

The signals between the SBus and LSC chip are described in Table 2-1. Note that the I/O column indicates the signal input or output direction from the SBus point of view. Also note that the signal names in these tables are the names used on the GX and GXplus schematic diagram.The pin-out for the 96-pin SBus connector used on the Single Chip card are shown in

Table 2-1 Signals Between SBus and LSC Chip

Name	Pin Number	I/O	Description
SBD<31..0>	See Table 2-2	I/O	SBus data signals
SBPA<23..0>	See Table 2-2	O	SBus physical address signals
SBSEL*	3	O	SBus Select signal indicating that this SBus slot is being selected by the CPU.
SBAS*	51	O	SBus Address Strobe signal used in conjunction with SBSEL* to validate signals on SBus.
SBSIZ<2..0>	27, 74, 26	O	Tells the LSC the size of the access being made by the CPU.
SBRD	75	O	SBus Read signal indicating a read when high and a write when low.
SBACK<2..0>*	44, 40, 36	I	SBus Acknowledgment signal from LSC chip to SBus. SBACK<1>*, SBACK<2>*, and SBACK<0>* are coded as follows:
SBCLK	49	O	SBus Clock signal to the LSC chip.
SBRESET*	95	O	SBus Reset signal 11, a reset from the SBus.

SBACK<2>*	SBACK<1>*	SBACK<0>*	FUNCTION
1	1	1	Idle/Wait
1	1	0	Error acknowledge
1	0	1	Byte data acknowlege
1	0	0	Rerun acknowledge
0	1	1	Word data ack.
0	1	0	Reserved
0	0	1	Half-word data ack.
0	0	0	Reserved

Table 2-1 Signals Between SBus and LSC Chip

Name	Pin Number	I/O	Description
SBIRQ5*	20	I	SBus Interrupt Request signal from LSC chip indicating that there is a vertical sync interrupt pending in the TEC section.
Vdd	56, 64, 72, 80, 88	PG	+5V power input
Ground	1, 52, 60, 68	PG	Ground

Table 2-2 SBus Connector Pinout

Pin Number	Description	Pin Number	Description	Pin Number	Description
01	GND	33	SBA <06>	65	SBD <18>
02		34	SBA <08>	66	SBD <20>
03	SBSEL*	35	SBA <10>	67	SBD <22>
04		36	SBACK <0>*	68	GND
05	SBD <00>	37	SBPA <12>	69	SBD <24>
06	SBD <02>	38	SBPA <14>	70	SBD <26>
07	SBD <04>	39	ABPA <16>	71	SBD <28>
08		40	SBACK <1>*	72	+5V
09	SBD <06>	41	SBPA <18>	73	SBD <30>
10	SBD <08>	42	SBPA <20>	74	SBSIZ <1>
11	SBD <10>	43	SBPA <22>	75	SBRD
12		44	SBACK <2>*	76	GND
13	SBD <12>	45		77	SBA <01>
14	SBD <14>	46		78	SBA <03>
15	SBD <16>	47		79	SBA <05>
16		48		80	+5V
17	SBD <19>	49	SBCK	81	SBA <07>
18	SBD <21>	50		82	SBA <09>
19	SBD <23>	51	SBAS*	83	SBA <11>
20	SBIRQ <5>*	52	GND	84	GND
21	SBD <25>	53	SBD <01>	85	SBPA <13>
22	SBD <27>	54	SBD <03>	86	SBPA <16>
23	SBD <29>	55	SBD <05>	87	SBPA <17>
24		56	+5V	88	+5V
25	SBD <13>	57	SBD <07>	89	SBPA <19>
26	SBSIZ <0>	58	SBD <09>	90	SBPA <21>
27	SBSIZ <2>	59	SBD <11>	91	SBPA <23>
28	SBIRQ <7>	60	GND	92	GND
29	SBA <00>	61	SBD <13>	93	

Pin Number	Description	Pin Number	Description	Pin Number	Description
30	SBA <02>	62	SBD <15>	94	
31	SBA <04>	63	SBD <17>	95	SBRESET*
32		64	+5V	96	

2.6 *Software Model*

The software controls the Single Chip GX card by reading and writing registers. These registers are located in seven data structures that control the corresponding parts of the card: EPROM, DAC, FHC, THC, FBC, TEC, and DFB. The following functions are performed by the indicated part of the card under software control:

TEC (Transformation Engine and Cursor control section):

- Transformation of an image from world coordinates to viewing coordinates using matrix mathematics
- Optional clip checking of the image against a unit perspective viewing pyramid (each of the six clipping planes may be individually enabled)
- Optional perspective division using matrix mathematics to project 3-D points onto the projection plane
- Optional transformation of the image (including scaling, rotation, and translation) using matrix mathematics into virtual device coordinates
- Transformation of the image into screen coordinates
- Optional autoloading of the transform results into the FBC
- General purpose vector mathematics
- Programmable monitor timing (sync, blanking, etc.)
- Programmable Video Memory timing control (refresh, transfer cycles)
- Display a programmable hardware cursor defined by a two-plane 32 × 32 pixel area

FBC (Frame Buffer Controller section):

- Drawing a point, line, triangle, or quadrilateral using a dual Bresenham algorithm to perform scan conversion into the frame buffer

- BLIT (block image transfer) a pixel-coordinate (COLOR8 mode) rectangular area in the frame buffer from a source location to a destination location with an optional RasterOp
- Font rendering of a precomputed image using character bit maps to (write) the frame buffer an image at a time. Images described in a single plane data structure can be written to the frame buffer in COLOR1 or HRMONO mode. Images described in an eight plane data structure can be written to the frame buffer in COLOR8 mode. For COLOR1 mode, the image is expanded to eight planes of data with the correct RasterOp and color. For HRMONO mode, the image is expanded to the proper grey scale values.
- Clipping of an image to make invisible any part of an object that is not in the viewing window.
- Picking of an object by clipping it to the viewing window without rendering. If any part of the object is in the window, the pick status bit is set
- Provides all VRAM address multiplexing for accelerated, Dumb Frame Buffer, and VRAM transfer cycles

Palette DAC:

- Read or write the color map
- Read or write the overlay map

2.6.1 Data Type

All data directly written to the TEC or FBC are 32-bit quantities. The FBC only deals with 32-bit integers. The TEC's data type is specified in the TEC `VDC_MATRIX` register. Note that the TEC math unit uses an internal format that is hidden from the user. The following data types are supported for TEC access and are externally visible:

- Single-precision IEEE floating-point: one sign bit, 8 exponent bits, and 23 fraction bits.
- Two's complement fixed point: 16 signed integer bits, and 16 fraction bits.
- Two's complement integer: 32 signed integer bits.

2.6.1.1 Minimum Driver Elements

The software driver for the GX card must contain the following elements:

- Code for reading the ID code and EPROM at boot time.
- Code for reading the forth code stored in the EPROM.
- Code for loading the Palette DAC.
- Code for initializing the TEC and FBC.
- Code for accessing the Dumb Frame Buffer (minimum function for console).

2.7 Global Address Map

The global address map shows the locations of the data structures for the various parts of the Single Chip GX card. Each of these locations is offset from the base address of the slot the card is installed in (`s4base`). The global ranges of the data structures are:

Part	Starting Address	Ending Address
ROM	s4base+0x000000	s4base+0x1FFFFF
DAC	s4base+0x200000	s4base+0x27FFFF
ALT	s4base+0x280000	s4base+0x280FFF
FHC	s4base+0x300000	s4base+0x300FFF
THC	s4base+0x301000	s4base+0x301FFF
FBC	s4base+0x700000	s4base+0x700FFF
TEC	s4base+0x701000	s4base+0x701FFF
DFB	s4base+0x800000	s4base+0xFFFFFF

The global offsets are:

```
rom   = s4base+0x000000
dac   = s4base+0x200000
alt   = s4base+0x280000
fhc   = s4base+0x300000
thc   = s4base+0x301000
fbc   = s4base+0x700000
tec   = s4base+0x701000
dfb   = s4base+0x800000
```

2.8 Local ROM Map

The map for the GX card's ROM is:

Starting	Ending

Word Address	Word Address	Function
rom+0x0000	rom+0x0003	SBus ID for GX card
rom+0x0004	rom+0x3fff	Boot Code

2.9 Local Palette DAC Map

The map for the GX card's Palette DAC is:

Starting Word Address	Read Function	Write Function
dac+0x0000	Read Address Register	Write Address Register
dac+0x0004	Read Color Palette	Write Color Palette
dac+0x0008	Read Control Register	Write Control Register
dac+0x000c	Read Overlay Color	Write Overlay Color

2.10 Local ALT Map

The ALT address space has been set aside for future expansion to access an additional external device to the LSC chip. This address space will be used for selecting the optional oscillators.

2.11 Local FHC Map

The FHC (FBC Hardware Configuration) register is not changed during normal operation. The information contained in the FHC register is shown on the *TurboGX Reference Card* (800–5112). The FHC map is:

Starting Word Address	Mnemonic	Function
fhc+0x0000	CONFIG	Configuration Register

2.12 Local THC Map

The THC (TEC Hardware Configuration) registers are not changed during normal operation; they are loaded by the boot PROMs during diagnostics. The information contained in each of the registers is shown in the *TurboGX Reference Card* (800–5112).

2.13 Local FBC Maps

The maps for the FBC section of the LSC along with the contents of the corresponding registers are documented in the *TurboGX Reference Card* (800–5112).

2.14 Local TEC Maps

The maps for the TEC section of the LSC along with the contents of the corresponding registers are documented in the *TurboGX Reference Card* (800–5112).

2.15 SBus Connector

The LSC card connects to the SBus on a Sun CPU board through a 96-pin male mini-DIN connector. This connector, J1, is used for both signal and power. The GXplus, which is a double-wide card, uses two of these connectors on the CPU board. The J1 connector is used for both signal and power. The J2 connector is used for power only. The LSC chip accepts commands and data through the 32-bit SBus data path and puts out the appropriate pixel information on the 64-bit pixel data path.

SBus Interface Block 3

This Chapter provides a functional description of the SBus Interface block of the LSC chip. Like the FBC and TEC, the SBus interface block is a major part of the LSC. The discussion here is limited to the internal functions of the LSC with reference to the SBus interface block.

3.1 SBus Interface Block Functions

The LSC chip provides an interface between the SBus and other components on the card. The LSC SBus interface block of the LSC chip performs the following functions:

- SBus handshaking for internal and external (to the LSC) SBus transfers
- Address decoding
- Timing synchronization between the SBus clock rate and the local board clock rate
- Buffering of SBus address, data and control signals for fast write capability
- Buffering of address, data and control signals for TEC to FBC transfers (autoload cycles)

These functions are described below in detail.

3.2 SBus Handshaking

The LSC chip interfaces with the SBus using the handshaking protocol described in Chapter 2, *SBus Interface*. An SBus Select signal (SBSEL*) along with an SBus Strobe signal (SBAS*) indicates that the Single Chip GX card is being selected. If the SBSIZ<2> signal is high, this indicates a burst transfer. The LSC does not support burst transfers and will return an error acknowledge to the SBus.

The SBus clock signal (SBCK) provides the basic timing for the SBus data transfers. All signals are sampled on the rising edge of this clock.

An SBus Reset signal (SBRESET*) resets the LSC chip. This signal resets to a known state.

The SBACK<2>*, SBACK<1>*, and SBACK<0>* signals provide transfer acknowledgment information to the SBus.

The LSC chip returns an SBIRQ5* signal to the SBus in response to a vertical sync interrupt pending in the TEC section.

3.3 Address Decoding

The LSC chip decodes the SBus Physical Address signals (SBPA<23..19, 12>) into appropriate "chip-select" signals. These signals are used to identify the various parts of the Single Chip GX card and internal sections of the LSC chip. The LSC address map is shown in Table 3-1.

Table 3-1 LSC Address Map

Function	**Bits Decoded**						**SBus Address Range**
	a23	**a22**	**a21**	**a20**	**a19**	**a12**	
CS_ROM (boot PROM)	0	**0**	**0**	**x**	**x**	x	0x000000 - 0x1fffff
CS_DAC (RAMDAC)	0	0	1	0	0	x	0x200000 - 0x27ffff
CS_ALT (Alternate Device)	0	0	1	0	1	0	0x280000 - 0x280fff
CS_FHC (FBC H/W Config.)	0	0	1	1	0	0	0x300000 - 0x300fff
CS_THC (TEC H/W Config.)	0	0	1	1	0	1	0x301000 - 0x301fff

Table 3-1 LSC Address Map

Function	Bits Decoded						SBus Address Range
	a23	**a22**	**a21**	**a20**	**a19**	**a12**	
CS_FBC (FBC)	0	1	1	1	0	0	0x700000 - 0x700fff
CS_TEC (TEC)	0	1	1	1	0	1	0x701000 - 0x701fff
SC_DFB (Dumb Frame Buffer)	1	x	x	x	x	x	0x800000 - 0xffffff

The CS_ROM, CS_DAC and CS_ALT are sent off-chip to external devices on the Single Chip GX cards. These external transfers happen synchronously with the SBus clock and no “syncing up” is required. The internal select signals (FHC, THC, FBC, TEC, and DFB) are synchronized with the internal clock which is based off of the input signal MAIN_OSC.

3.4 *Buffering and Pipelining*

SBus address, data, and control signals are buffered, and for a write transfer, an immediate acknowledge is given back to the SBus master performing the write. The signals are then synchronized internally and the write eventually completes with an internal acknowledge being returned to the SBus Interface control logic from the selected address space. Reads must wait for the data to become available which is signalled by the appropriate internal acknowledge. This acknowledge is then resynced to the SBus clock and used to send the SBus acknowledge to end the transfer.

A two stage buffer is used internally to accept SBus address, data and control signals and acknowledge the SBus transfer as quickly as possible. SBus writes always complete in three SBus clock cycles provided the top buffer is empty.

SBus reads from the internal sections of the LSC take between 5 and 7 SBus clock cycles when the chip is idle. The buffer is also used for TEC to FBC transfers (autoload cycles).

3.5 ROM Transfers

The ROM address space is used to access the Single Chip GX card's on-board boot PROM. Transfers to this space will always be acknowledged with an 8-bit acknowledge (SBACK<2..0> = 5). Writes are allowed in the sense that the SBus acknowledge occurs but the external signal CS_ROM* remains inactive. Reads to this space will cause an 8 SBus clock cycle output on the CS_ROM* pin. This timing is designed for 250 nsec or faster PROMs.

Figure 3-1 shows the ROM space read cycle.

Figure 3-2 shows the ROM space write cycle.

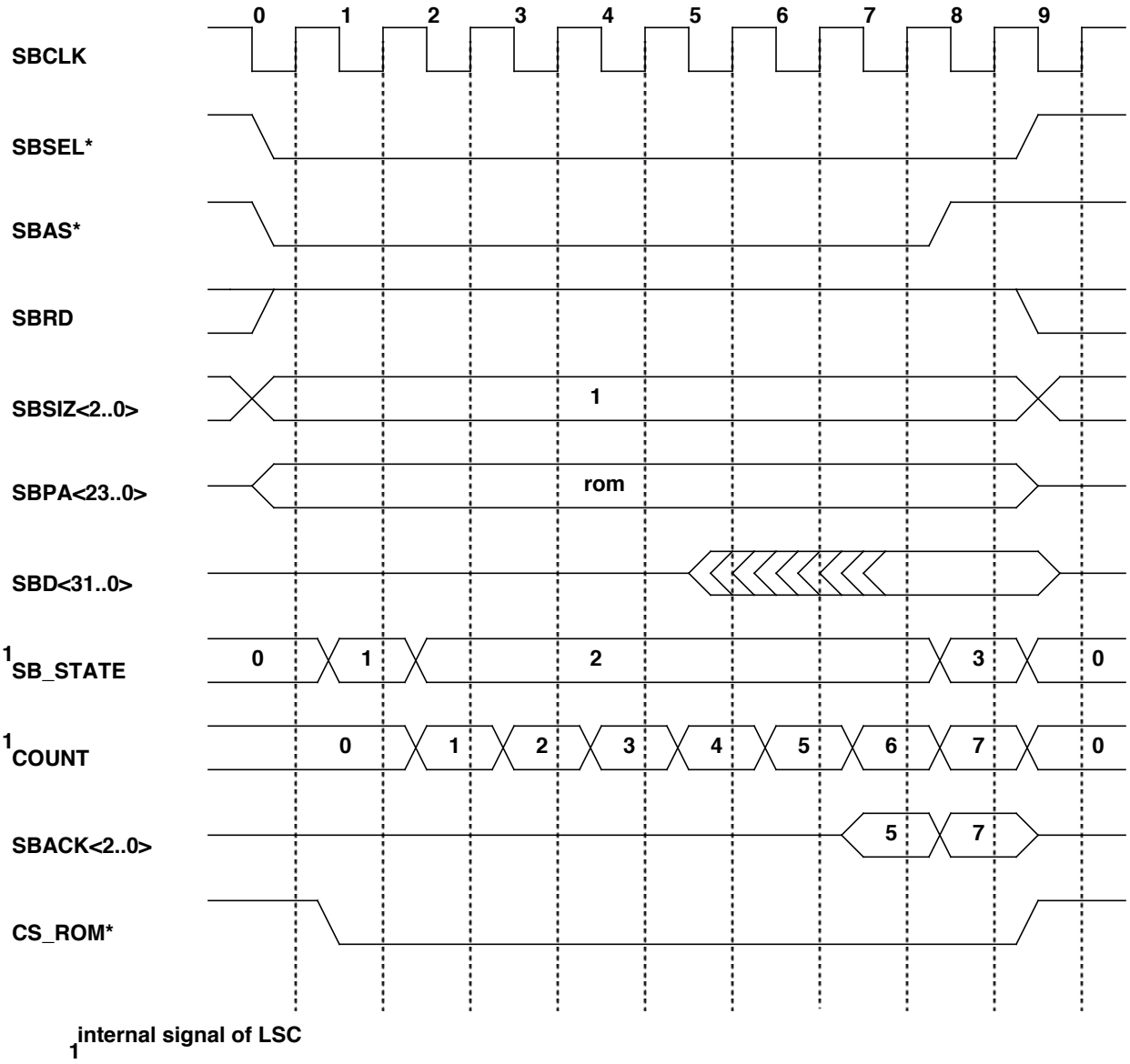
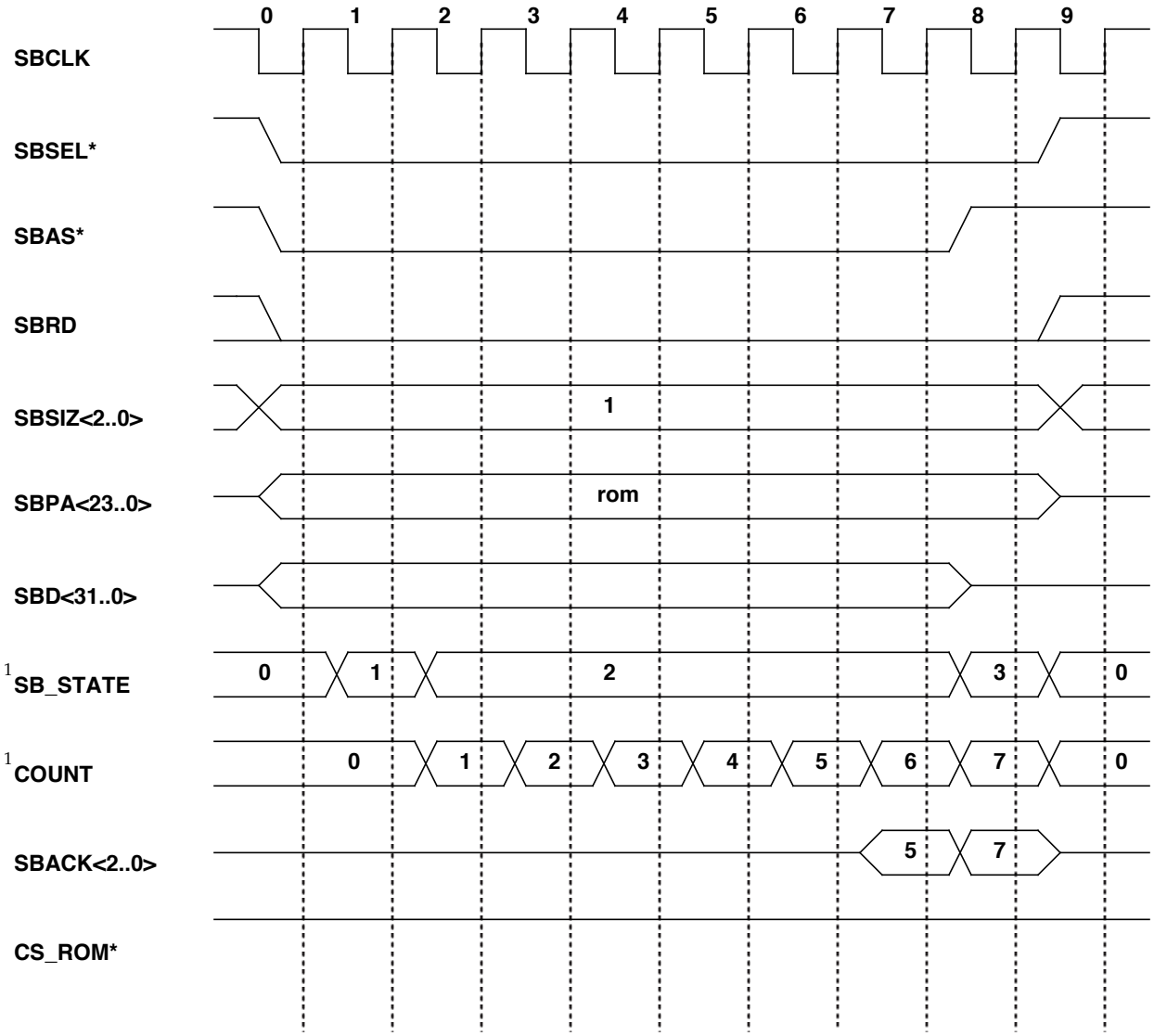


Figure 3-1 ROM Space Read Cycle



[1]internal signal of LSC

Figure 3-2 ROM Space Write Cycle

3.6 DAC Transfers

The DAC address space is used to access the registers in the Single Chip GX card's RAMDAC. This address space is treated as a 32-bit port on the SBus and will always acknowledge with a 32-bit acknowledge (SBACK<2..0> = 3). Only the upper byte (SBD<31..24>) is used on the Single Chip GX cards to map into the 8-bit port of the RAMDAC. Transfers happen synchronously with the SBus clock, with writes and reads both taking 4 SBus clock cycles. The timing is designed for a Brooktree Bt458 or compatible part.

Figure 3-3 shows the DAC space read cycle.

Figure 3-4 shows the DAC space write cycle.

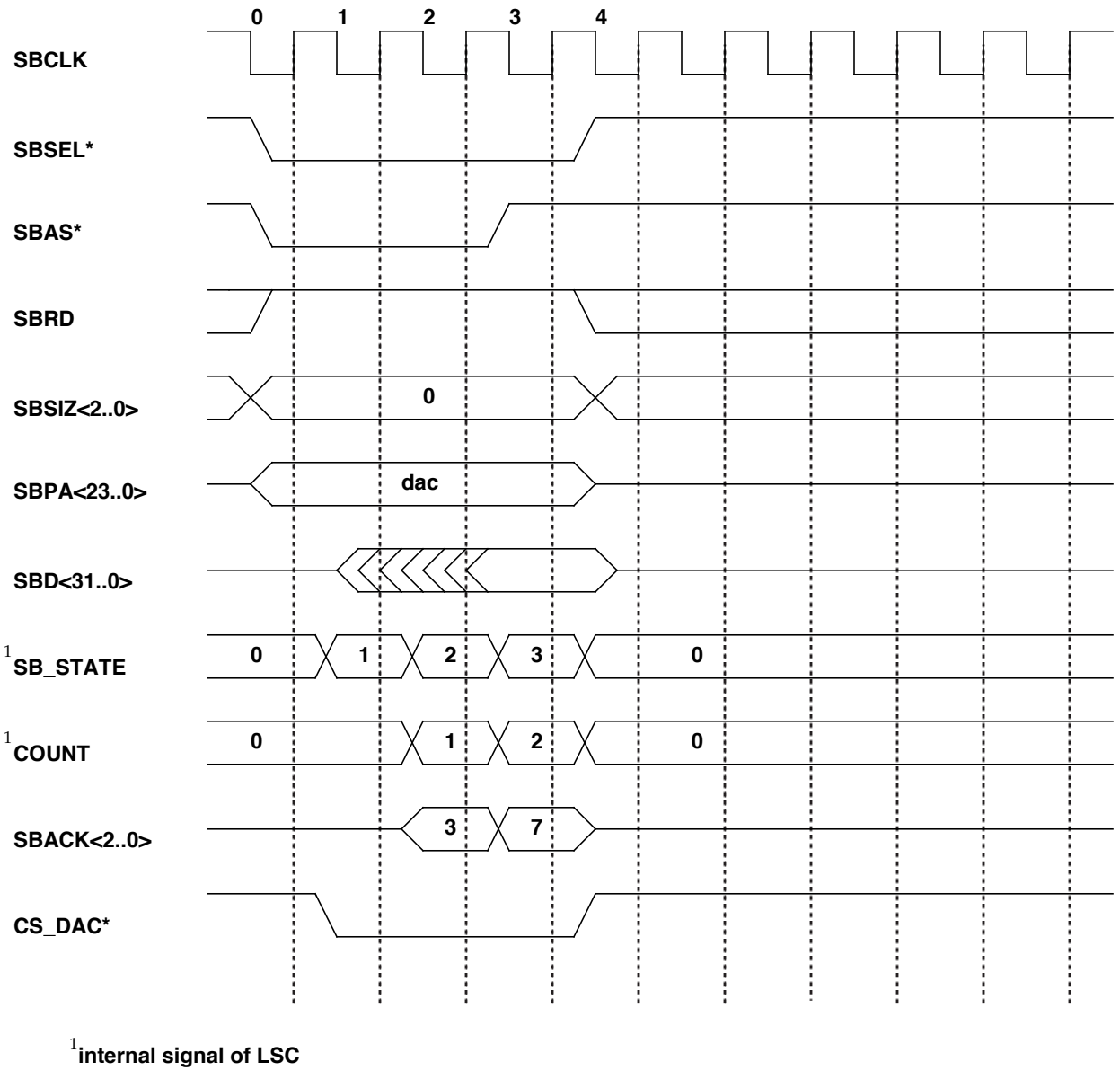
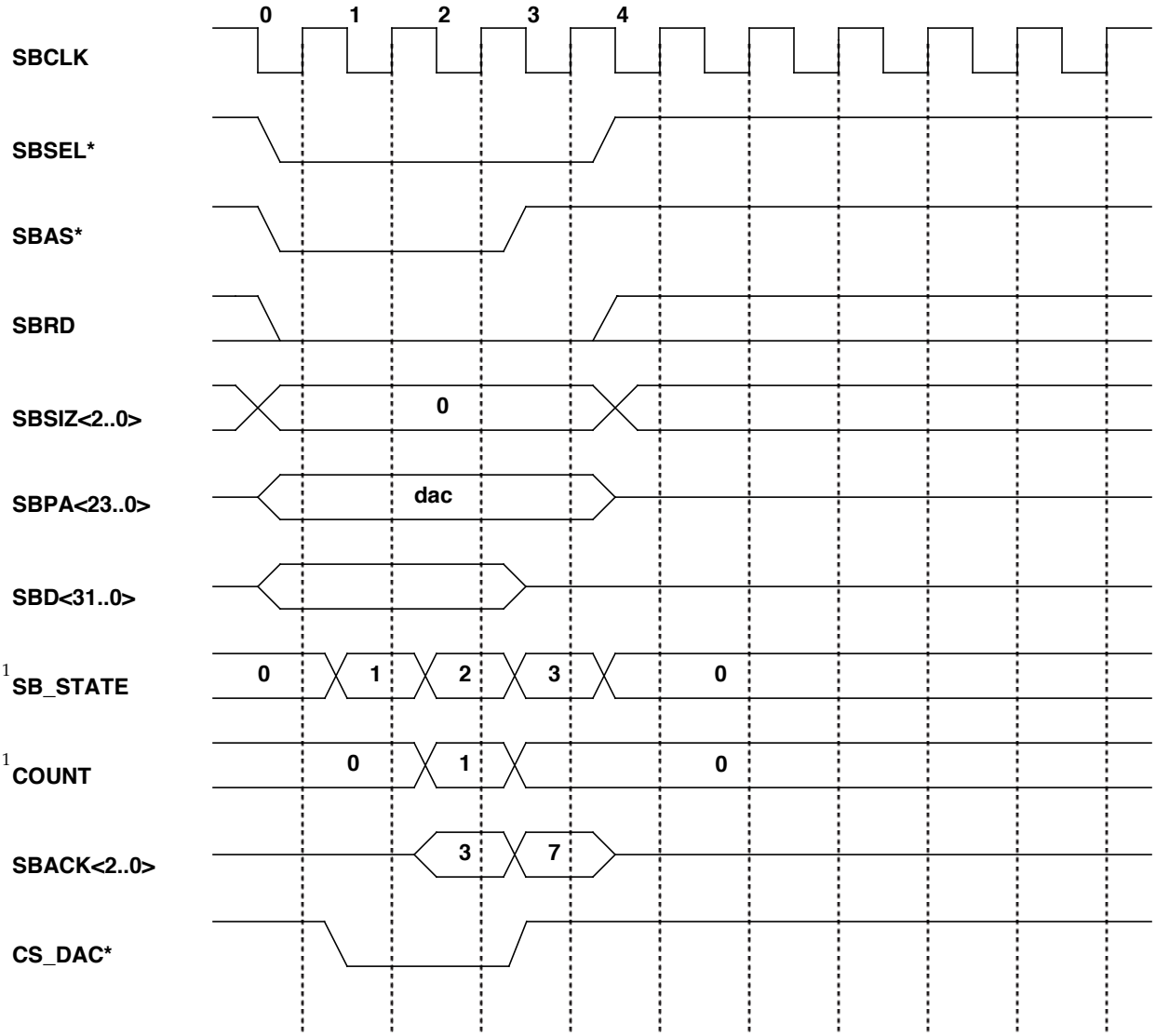


Figure 3-3 DAC Space Read Cycle



[1]internal signal of LSC

Figure 3-4 DAC Space Write Cycle

3.7 ALT Transfers

The ALT address space is used as a synchronous, 32-bit port with writes and reads both taking 5 SBus clock cycles. On the GXplus, it selects the oscillator to be used for video timing. On the TurboGX, it accesses the frequency generator.

Figure 3-5 shows the ALT space read cycle.

Figure 3-6 shows the ALT space write cycle.

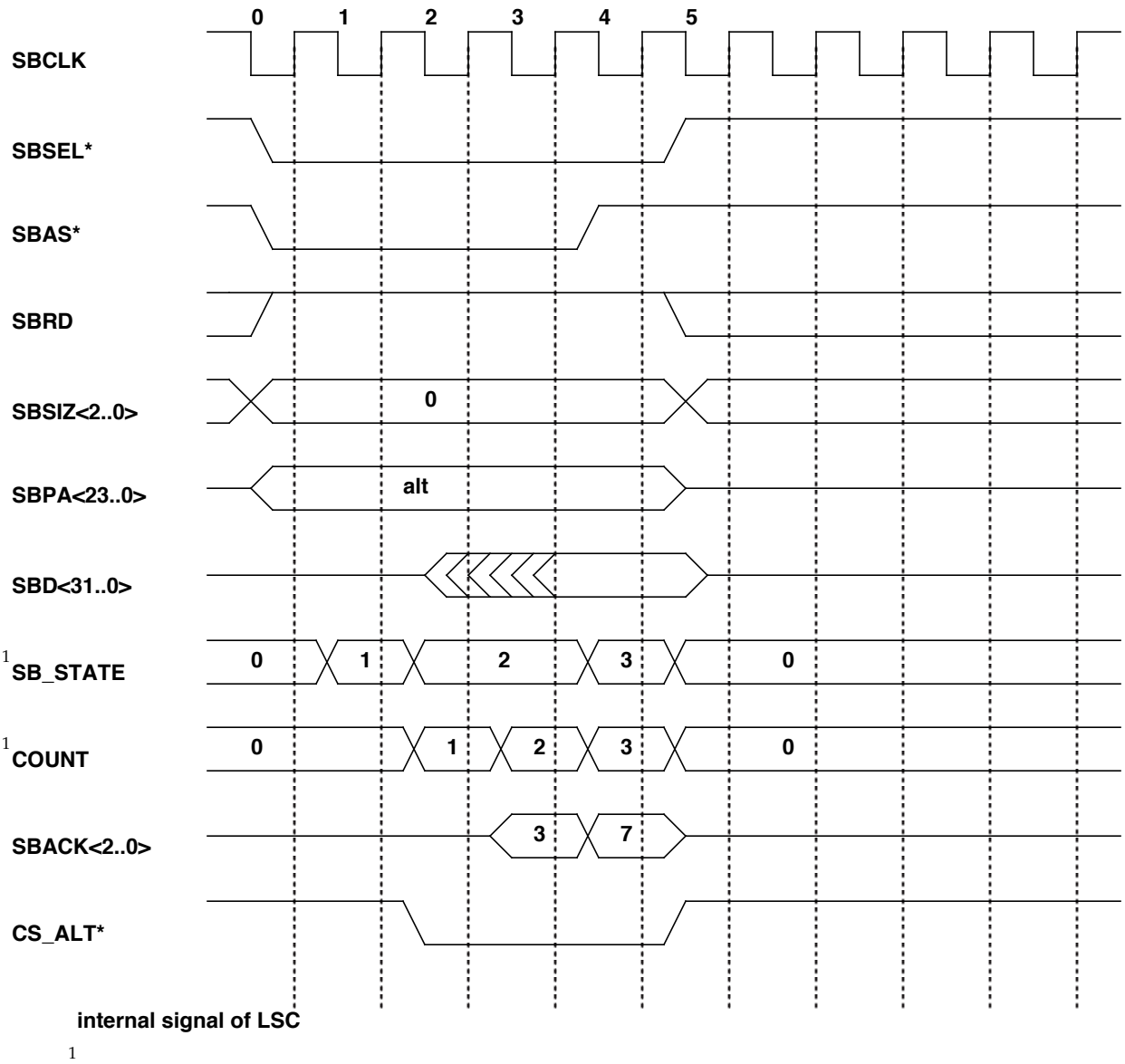


Figure 3-5 ALT Space Read Cycle

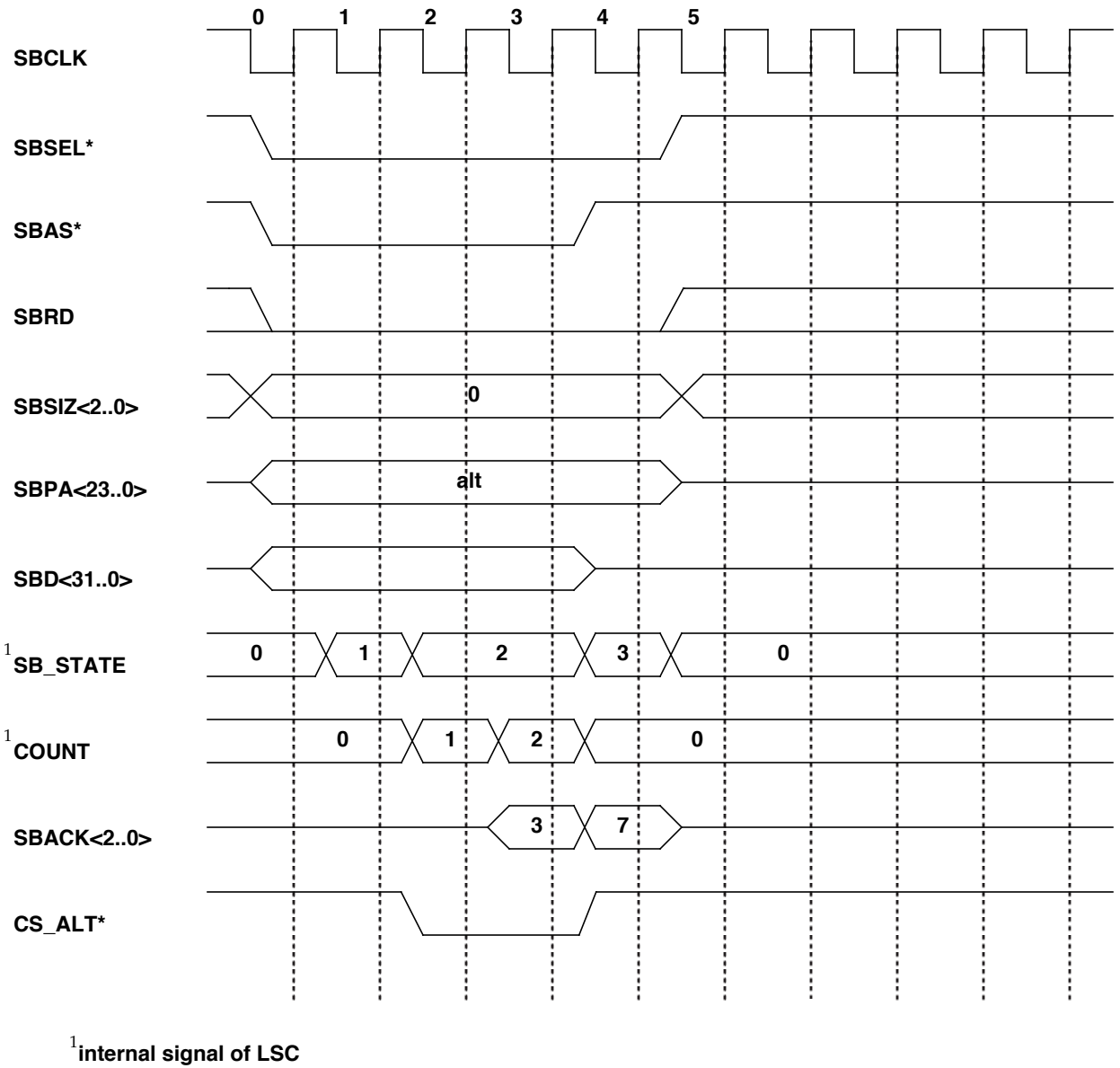


Figure 3-6 ALT Space Write Cycle

3.8 FHC/FBC Transfers

The FHC and FBC address spaces map into the FBC section of the LSC chip. This space is a 32-bit port and transfers must sync up to the local clock internal to the LSC chip. Because of the buffering feature described earlier, writes always immediately acknowledge and take 3 SBus clock cycles to be acknowledged as long as the pipeline is not full. When the chip is idle, a read will take 5 or 6 SBus clock cycles to acknowledge, based on the speed of the SBus clock and the relative clock skew between the SBus clock and the internal clock of the LSC chip.

Figure 3-7 shows the FHC/FBC space read cycle.

Figure 3-8 shows the FHC/FBC space write cycle.

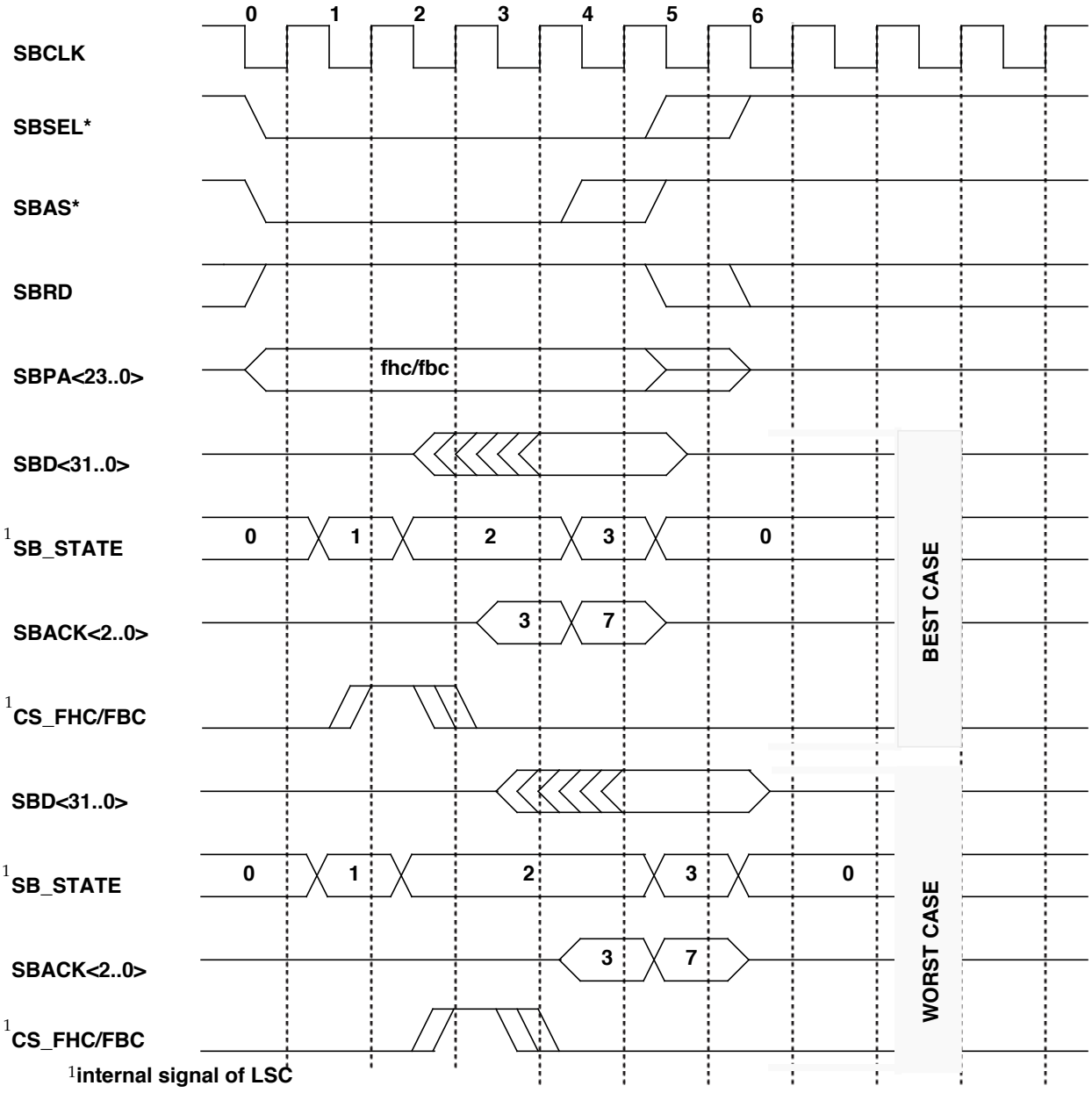
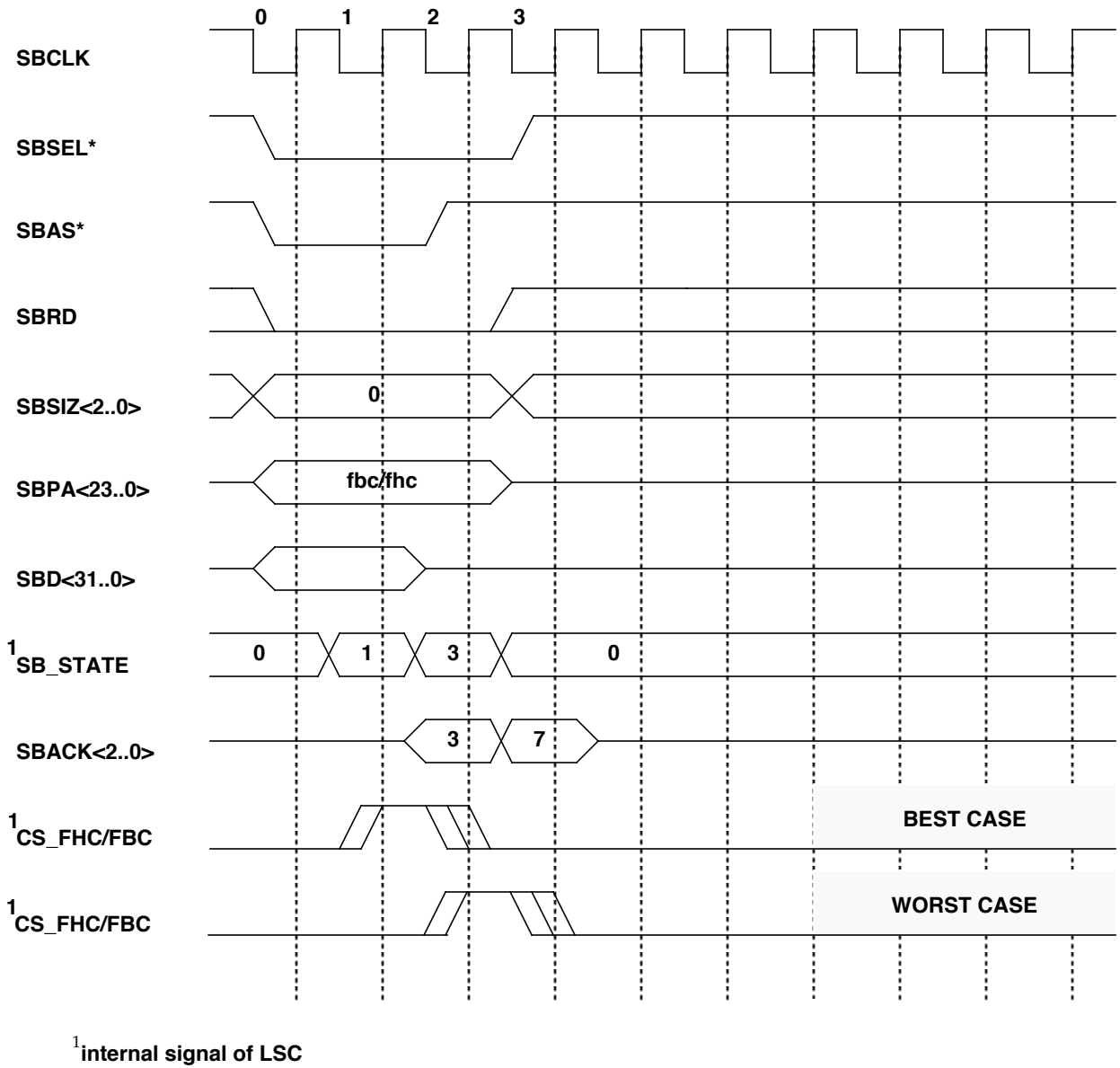


Figure 3-7 FHC/FBC Space Read Cycle



[1]internal signal of LSC

Figure 3-8 FHC/FBC Space Write Cycle

3.9 THC/TEC Transfers

The THC and TEC address spaces map into the TEC section of the LSC chip. This space is a 32-bit port and transfers must sync up to the local clock internal to the LSC chip. For the reasons mentioned above, writes will take 3 SBus clock cycles and reads will take 5 to 7 SBus clock cycles to acknowledge.

Figure 3-9 shows the THC/TEC space read cycle.

Figure 3-10 shows the THC/TEC space write cycle.

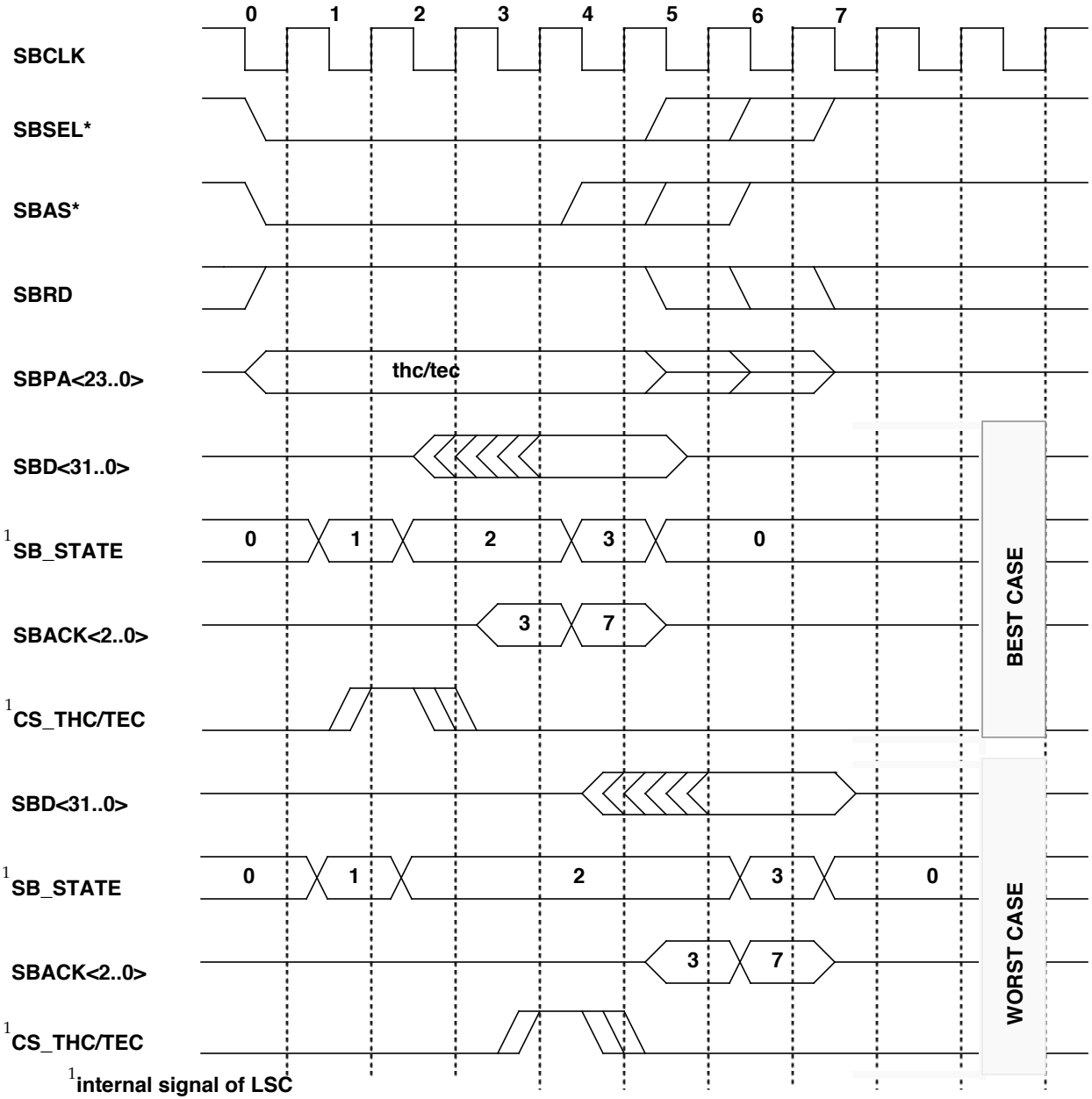


Figure 3-9 THC/TEC Space Read Cycle

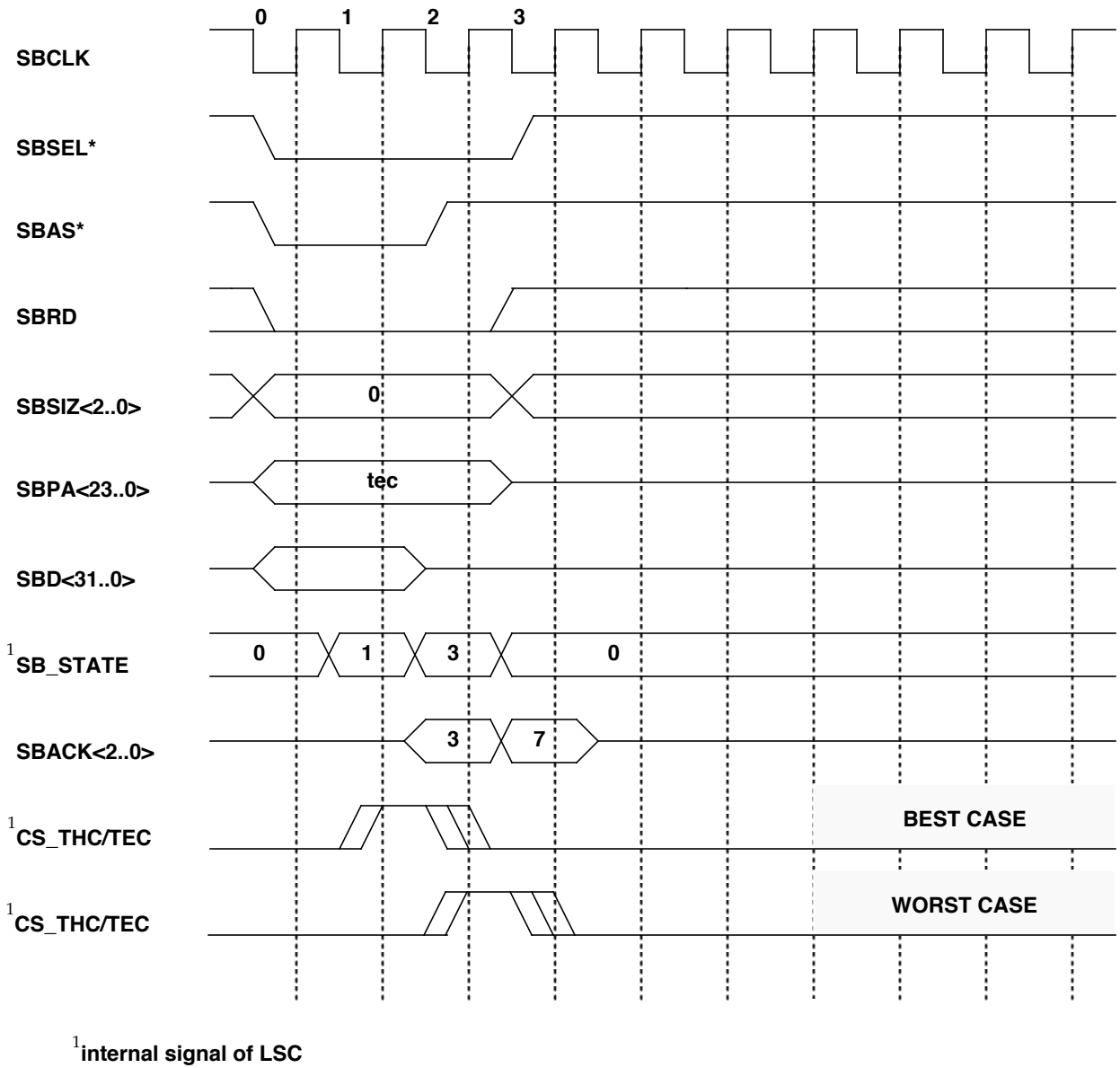


Figure 3-10 THC/TEC Space Write Cycle

3.10 DFB Transfers

The DFB address space maps into the memory control section of the LSC chip. The FBC section of the LSC helps generate the correct address and is involved in the transfer along with the memory control section. This space is a 32-bit port and transfers must sync up to the local clock internal to the LSC chip. For the reasons mentioned above, writes will take 3 SBus clock cycles and reads will take 5 or 6 SBus clock cycles to acknowledge when the LSC is idle. It may take up to 12 cycles to acknowledge a dumb frame buffer read if the LSC is busy.

Figure 3-11 shows the DFB space read cycle.

Figure 3-12 shows the DFB space write cycle.

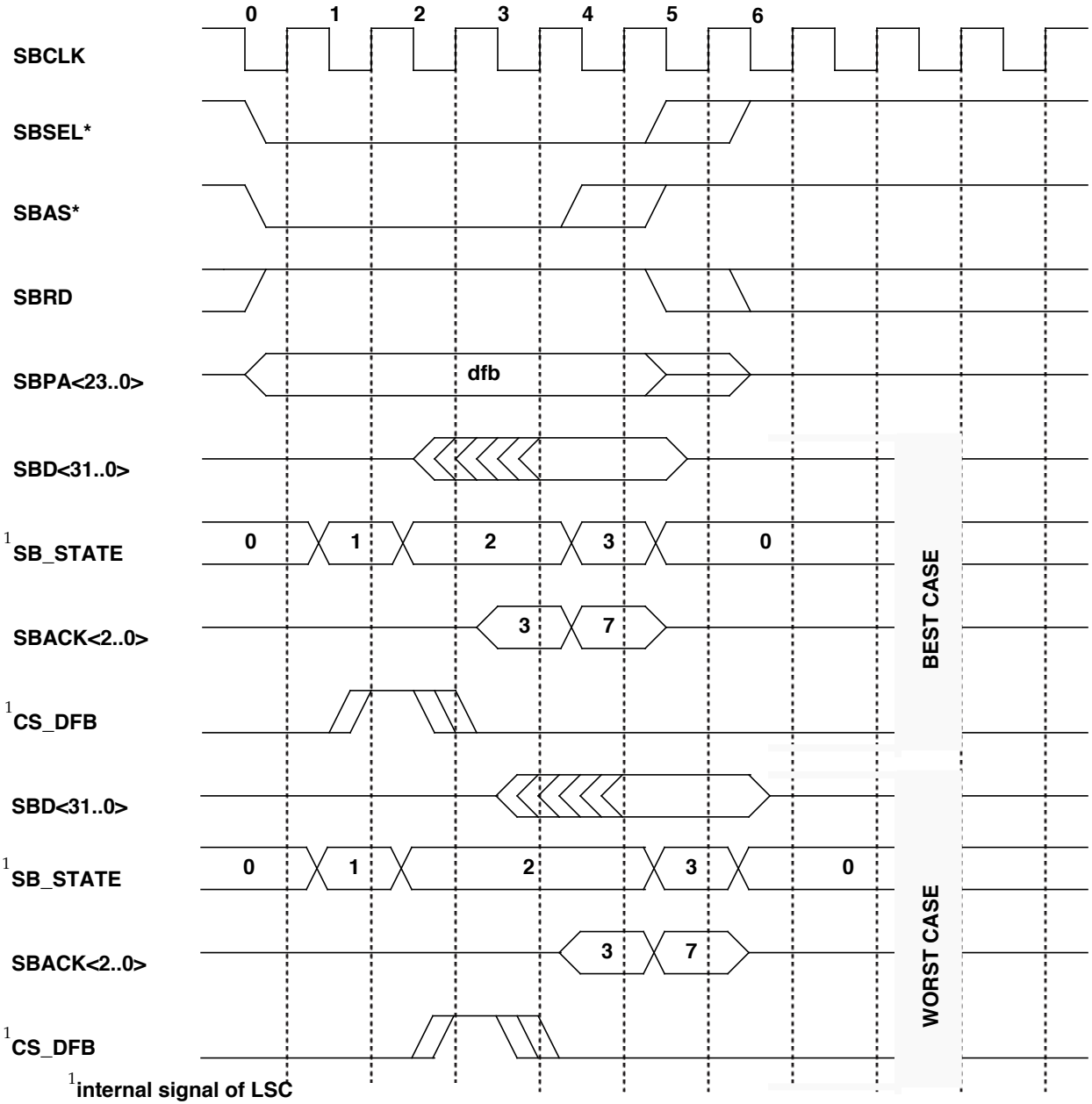
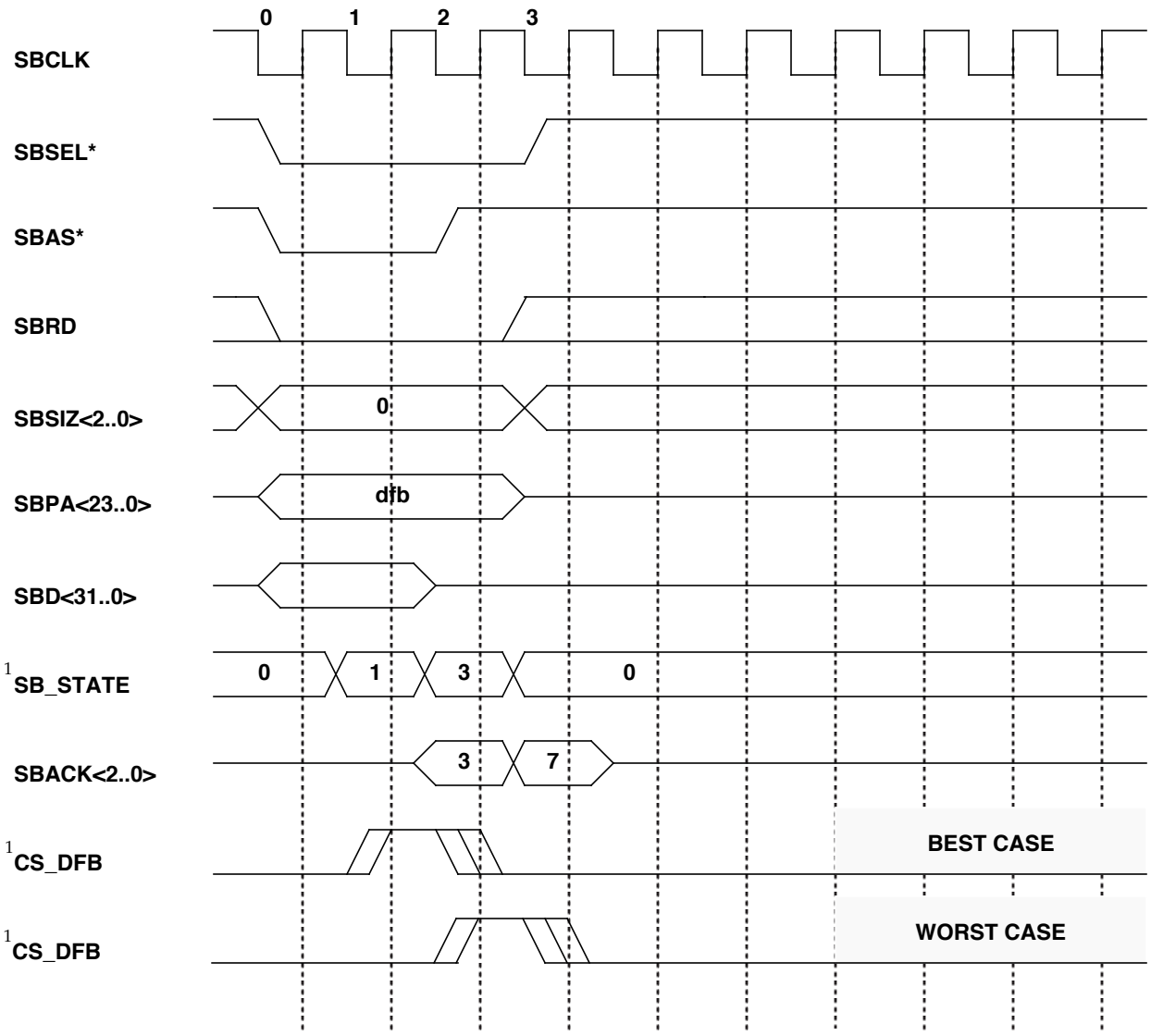


Figure 3-11 DFB Space Read Cycle



[1]internal signal of LSC

Figure 3-12 DFB Space Write Cycle

LSC Core 4

This chapter describes the core of the LSC Graphic Accelerator card along with hardware information about the chips that include signal descriptions, handshaking protocol, and timing information. The core consists of the TEC (Transformation Engine and Cursor) block, the FBC (Frame Buffer Controller) block, and memory controller.

Figure 4-1 shows the LSC chip configuration.

The graphic operations accelerated by the GX, GXplus, TurboGXplus, and TurboGX cards are divided between two blocks: TEC and FBC. The TEC block transforms 2-D and 3-D coordinates and provides a programmable hardware cursor. In addition, it controls timing of the video memory and the video signals that drive the monitor. The FBC block renders graphic objects into the video memory.

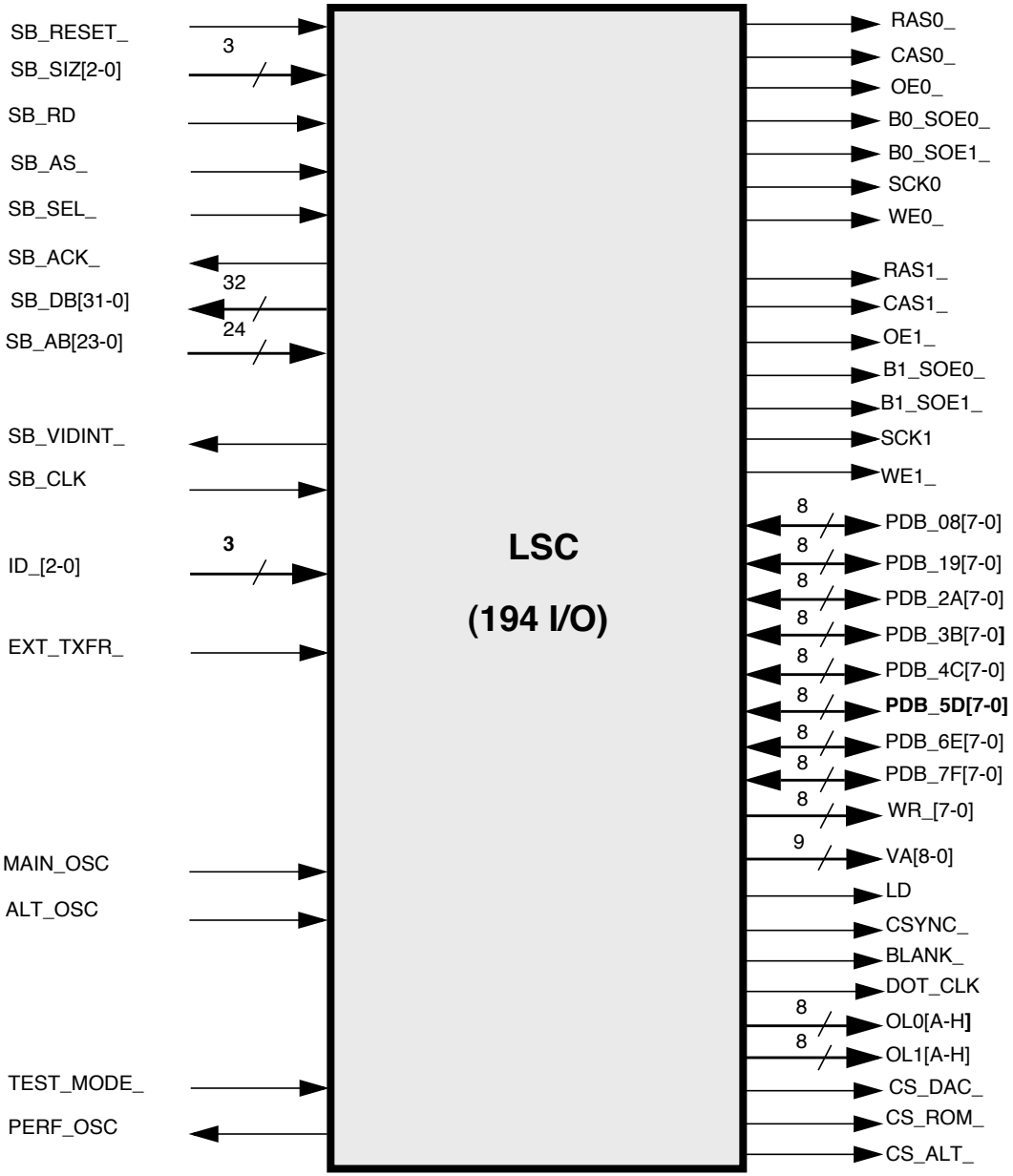


Figure 4-1 LSC Chip Configuration Diagram

4.1 LSC Signal Descriptions

All the signals associated with LSC are described below in detail.

Symbol	Type	Description
SB_CLK	I	SBus clock. This pin provides the basic timing for the LSC's SBus interface logic. It should run in the 16–25 MHz range and should be symmetrical. This pin has Schmidt trigger TTL input and an internal pullup.
SB_RESET	I	Bus reset. In general, this input causes the LSC to reset to a known state. However, its usage is qualified with the state of the TEST_MODE_ input. The effect of SB_RESET_ can be identified from the following table.

Table 4-1 SB_RESET_ in TEST_MODE_

TEST_MODE_	SB_RESET_	Characteristics
0	0	Enable scan chain shifting, force main_osc==clk2x==clk, force_main_osc==ld_clk2x==ld_clk, select scan output on PERF_OSC, reset (clear) THC STRAP register, ID_ [0]=scan input, ID_ [1]=scan enable
0	1	Tristate all outputs, force main_osc==clk2x==2*clk, force main_osc==ld_clk2x==2*ld_clk, select Param. Nand tree on PERF_OSC, reset (clear) THC STRAP register.
1	0	known state, Select Param. Nand tree on PERF_OSC_.
1	1	Normal functional mode, select performance osc on PERF_OSC.

Note – clk, clk2x, ld_clk2x, and ld_clk are LSC internal signals.

		When the TEST_MODE_==1, SB_RESET_ is assumed to be synchronous to SB_CLK. When TEST_MODE_==0, SB_RESET_ is assumed synchronous with MAIN_OSC. This pin has a Schmidt trigger TTL input and an internal pullup.
SB_SIZ[2-0]	I	SBus size. These inputs tell the LSC the size of the access being made by the SBus. These lines are only used when SB_SEL_ and SB_AS_ are active. The LSC will return an error if the SB_SIZ lines indicate that a BURST cycle has been requested. These pins have internal pullups.
SB_RD	I	SBus RD. This input tells the LSC whether the SBus's request is read (high) or write (low). This pin has an internal pullup.
SB_AS_	I	SB Address Strobe. This input indicates that the SBus address, data, and control signals are valid on the SBus. This pin has an internal pullup.
SB_SEL_	I	SBus slave Select. This input indicates that the SBus is selecting the LSC for access. This pin has an internal pullup.
SB_ACK_[2-0]	O	SBus transfer acknowledge. These outputs indicate the conclusion of an LSC SBus transaction. These lines are normally tristate and get driven actively for only the concluding two cycles of an LSC SBus access. Refer to SBus Specification (P/N 800-4453).
SB_VIDINT_	O	SBus interrupt for VBLANK event. This open-drain output indicates that the LSC is requesting an SBus interrupt to indicate that occurrence of a vertical blanking event.
SB_DB[31-0]	I/O	SBus data bus. These pins contain data being transferred between the LSC and the SBus. These pins have internal pullups.
PDB_xx[7-0]	I/O	Pixel data bus. These pins are bidirectional data lines that transfer data to and from the VRAM memory. Table 4-2 shows how the data lines

should be connected. In this table, the pixel 0 is the leftmost pixel and pixel 7 is the rightmost pixel. These pins have internal pullups.

Table 4-2 Data Lines Connections for Pixel Data Bus

Data	Bank 0	Bank 1 (only for double buffer board
PDB_08	Pixel 0	Pixel 0
PDB_19	Pixel 1	Pixel 1
PDB_2A	Pixel 2	Pixel 2
PDB_3B	Pixel 3	Pixel 3
PDB_4C	Pixel 4	Pixel 4
PDB_5D	Pixel 5	Pixel 5
PDB_6E	Pixel 6	Pixel 6
PDB_7F	Pixel 7	Pixel 7

Symbol	Type	Description
WR_[7-0]	O	Write Enable. These outputs are used to enable individual pixels during VRAM write cycles. All WR_ signals are driven low when the row address is on the address bus for loading the plane mask into the video RAMs.
WE0_	O	Bank 0 Write enable: Only intended for use in double buffered H/W applications, this output should be logically ANDed with the WR_ outputs and its results can be used to drive Bank 0 VRAM WR inputs.
WE1_	O	Bank 1 write enable. Only intended for use in double buffered H/W applications. This output should be logically ANDed with WR_ outputs and its results can be used to drive Bank 1 VRAM WR inputs.
VA[8-0]	O	VRAM address. These outputs can be used to drive the multiplexed VRAM address inputs directly. The linear address bits that appear on the VA output bus is a function of the memory control operation and the type of VRAM utilized

(indicated in the THC address space's STRAP register). The usage of the VA lines is described in the following table.

Table 4-3 VA Lines Usage

Control Operation	**128K x 8**	**256K x 4**
normal RAS	LA[19-11]	LA[20-12]
normal CAS	LA[11-4], B	LA[11-4], B
transfer RAS	TA[8-0]	TA[8-0]
transfer CAS	0s	0s

Legend:

LA[xx] refers to linear address bits.

TA[xx] refers to the transfer address counter.

B refers to internally generated interleave select bit.

RAS0,_CAS0_OE0	O	Bank 0 VRAM control. In single buffered H/W applications, these outputs are intended to drive the VRAM control inputs. In double buffered H/W applications, these outputs should drive just BANK 0 VRAM control inputs.
RAS1_CAS1_OE1	O	Bank 1 VRAM control. In single buffered H/W applications, these outputs are not used. In double buffered H/W applications, these outputs should drive just BANK 1 VRAM control inputs.
SCK0	O	Bank 0 serial shift clock. In single buffered H/W applications, this output is intended to drive the VRAM shift clock inputs. In double buffered H/W applications, this output should drive just BANK 0 VRAM shift clock inputs. This output is synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
SCK1	O	Bank 0 serial shift clock. In single buffered H/W applications, this output is not used. In double buffered H/W applications, this output should drive just BANK 1 VRAM shift clock inputs. This

		output is synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
B0_SOE0_	O	Bank 0 VRAM Serial Data Output Enable 0. In hardware applications with a 4-pixel wide DAC B0_SOE0_ and B0_SOE1_ alternate for each shift clock to multiplex 8 pixels down into the 4-pixel DAC input. In hardware applications with an 8-pixel wide DAC, B0_SOE0_ and B0_SOE1_ are both low continuously. Single buffered hardware applications use only B0_SOE0_ and B0_SOE1_. These outputs are synchronous within the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
B0_SOE1_	O	Bank 0 VRAM Serial Output Enable 1. See B0_SOE0_ above.
B1_SOE0_	O	Bank 1 VRAM Serial Output Enable 0. This output as well as B1_SOE1_ are the serial output enables for the 2nd bank in double buffer hardware applications. B1_SOE0_ and B1_SOE1_ alternate on each shift clock when bank 1 is being displayed. They remain high when bank 0 is displayed.
B1_SOE1_		Bank 1 VRAM Serial Output Enable 1. These outputs are synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation. See 1_SOE0_ description above.
CSYNC_	O	Composite Sync: This output is the combined sync signal for use by the monitor. This output is synchronous with the oscillator input (MAIN OSC or ALT_OSC) selected for video timing generation.
BLANK_	O	Blank. This output is the blanking signal for the video DACs. This output is synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.

OLA[A-H]	O	Overlay plane 0. These outputs are for plane 0 of the hardware cursor. Groups of four planes use OL0[A-H]. Bit A is the leftmost pixel. These outputs are synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
MAIN_OSC	I	Main LSC oscillator input. This oscillator input (or binary divisions of it) are used to clock the core logic of the LSC and its RAS/CAS/OE memory timing. It can also be selected to provide the basic video timing control and thus be used to generate the DOT_CLK and LD clocks and related synchronous signals. The intended frequency of MAIN_OSC is either 92.9405 MHz or 46.47025 MHz. This signal has a Schmidt trigger TTL input with an internal pull-up.
ALT_OSC	I	Alternative oscillator input. It can be selected to provide the basic video timing control and thus be used to generate the DOT_CLK and LD clocks and related synchronous signals. The maximum frequency of ALT_OSC is 117 MHz. This signal has a Schmidt trigger TTL input with an internal pull-up.
DOT_CLK	O	Video dot clock. This output can be selected via the THC address space STRAP register to reflect either the MAIN_OSC or ALT_OSC input.
LD	O	Load clock. This output is derived from the oscillator input selected to generate the DOT_CLK output. This output can be a divide-by-4 or a divide-by-8 of the DOT_CLK frequency depending on the DAC_MUX setting in the THC address space STRAP register.
CS_DAC_	O	DAC chip select. This output is asserted low when the LSC detects an SBus access intended for the DAC.

CS_ROM_	O	ROM chip select. This output is asserted low when the LSC detects an SBus access intended for the DAC.
CS_ALT_	O	Alternate chip select. This output is asserted low when the LSC detects an SBus access intended for an external device accessed through the alternate device address space.
ID_[0-2]	I	Identification. These inputs contain the identification code for the frame on which these chips are installed. This code shows up in the LSC's CONFIG register within the FBC/FHC address space. These pins have internal pullups. Whenever _MODE_== 0), ID[0] is used as the (uncomplemented) serial scan chain input. ID[1] is used as a high-true scan chain shift enable.
EXT_TXFR_	I	External Transfer: When enabled by the EXT_TRANSFER bit in the LSC STRAP register bit, this input indicates to the LSC that an external memory controller is requesting a transfer cycle. The leading (rising) edge is synchronized and fed to the memory control arbitration logic instead of the transfer signal generated by the LSC timing generation logic. Transfer cycles are given the highest priority and are thus guaranteed service once memory accesses already in progress are concluded. The EXT_TXFR signal needs to be asserted for a minimum time greater than or equal to 13 clk1x periods (551 ns if the FBC is running at 23.24 MHz). The trailing (falling) edge of EXT_TXFR will, as a combination, cause the deassertion (rising edge) of OE0_ and OE1_ thus completing a transfer cycle. Note, the LSC will always reset its transfer address counter to 0 during VBLANK. An external transfer address should be multiplexed in with the VA[8-0] generated by the LSC. This input has an internal pull-up.

TEST_MODE_	I	Test mode. This input along with the SB_RESET_ input determines which functional or testing mode the LSC is in. Refer to the table in the SB_RESET_ description for details. This signal has a Schmidt trigger input and external pullup.
PREF_OSC	O	Performance oscillator. This output has different meanings depending upon the state of TEST_MODE_ and SB_RESET_. See the table below for details.

Table 4-4 TEST_MODE_ and RESET_ States

TEST_MODE_	SB_RESET_	Characteristics
0	0	select scan chain output
0	1	select Parametric NAND tree
		select Parametric NAND tree
		select performance Oscillator

When selected as the performance oscillator output, a square wave with an approximate frequency of 2.5 MHz should be present. Compare the output of this frequency with Table 4-5 to determine the relative timing performance of the device versus simulation at best case, typical, and worst case commercial conditions.

Table 4-5 Timing Performance of the Device (Testing in progress data is to be defined)

Condition	Frequency	Period
Best case	-	-
Typical	-	-
Worst case	-	-

4.2 Testing Methodology

The testing methodology for the LSC utilizes three basic approaches: partial scan, parallel functional access, and special test modes for achieving the targeted fault coverage (>95%) requirement. The approaches used for each of the major modules comprising the LSC are:

CLOCK_GEN: Fault coverage via normal functional patterns

FBC_CORE:	Fault coverage via normal functional patterns and partial scan (90%+ of flip-flops scanned).
TEC_CORE	Fault coverage via normal functional patterns and scan only for signals provided to the FBC_CORE.
MCTRL_LOGIC	Partial scan (50%+ of flip-flops scanned)
SBUS_LOGIC	Partial scan (90%+ of flip-flops scanned)

Partial (as opposed to full scan) has been used throughout the design due to the usage of some negative edge, 2x speed flip-flops, as well as the need to reduce the design size. The design also contains numerous latch-based storage elements. These elements are maintained in a transparent mode while the design is in scan test mode. Non-scanned flip-flops are either prevented from changing state while shifting in/out scan patterns or are prevented (or isolated) from affecting scannable circuitry while the LSC is in scan test mode.

One type of scan employed by the LSC is a single scan chain with a common single-edged clock (same clock that is used in functional mode) with a global scan-shift enable pin/signal.

The scannable portions of the chip are to be tested via functional patterns and ATPG patterns. The non-scannable portions of the chip are to be tested via functional patterns only.

Note, the design will use ~80K parallel test vectors in addition to the ATPG-generated serial scan vectors. The scan chain is approximately 1134 elements long.

Also included in the design is a free-running internally-generated oscillator (PERF_OSC) that is accessible at a pin on the chip. The period of this oscillator should directly reflect the AC performance characteristics of the LSC's core logic.

Table 4-6 shows the dc parameters. Table 4-7 shows the pin loading assumptions.

Table 4-6 DC Parameters

Parameter	Signals	Conditions	Min	Max	Unit
Voh	PERF_OSC	Ioh =-1mA	2.4		V
Voh	LD, CS_xxx CSYNC_,BLANK_ OL0[A-H], OL1[A-H], WEx_	Ioh = -2mA	2.4		V
Voh	PDB, SB_DB,	Ioh = -4mA	2.4		V
	WR_[7:0], DOT_CLK, Bx_SOEy_		2.4		V
Voh	RASx_, CASx_, OEx_,SCKx, VA	Ioh = -6mA	2.4		V
Voh	SB_ACK_[2:0]	Ioh = -8mA	2.4		V
Voh	PERF_OSC	Iol = 1mA	0.8		V
Voh	LD, TXD, CS_xxx, CSYNC, BLANK_ OL0[A-H], OL1[A-H], WEx_	Iol = 2mA	0.8		V
Vol	PDB, SB_DB, WR_[7:0], Bx_SOEy_, SB_VIDINT_*,DOT_CLK	Iol - 4mA	0.8		V
Vol	RASx_, CASx_, OEx_, SCKx, VA	Iol = -6mA	0.8		V
Vol	SB_ACK_[2:0]	Iol= - 8mA	0.8		V
Vih				0.8	V
Vil			2.4		V
Li	All inputs	0 < VI < Vcc	50	100	uA
Ri	All inputs	input pullup	50K	100K	Ohms
Vcc			4.75	5.25	V
Icc				~300	mA
Ci	All inputs			12	pF

*Open drain output

Table 4-7 Pin Loading Assumptions

Output	Loading
PERF_OSC	10pF
VA[8:0]	100pF
RASx_	120 pF
CASx_	120 pF
OEx_	120 pF
B0_SOEx_	60 pF
B1_SOEx_	60 pF
SCKx	120 pF
WR_[7:0]	40 pF
WEx_	50 pF
SB_DB[23:0]	160 pF
SB_ACK[2:0]	120 pF
PDB_xx[7:0]	30 pF
SB_VIDINT_	120 pF
CSYNC_	15 pF
BLANK_	15 pF
LD	15 pF
DOT_CLK	20 pF
OL0[A-H]	15 pF
Ol1[A-H]	15 pF
CS_XXX_	25 pF
SB_RESET	120 pF

4.3 LSC Packaging

The LSC is in a 223-pin package in a 18 x 18 grid of pins numbered linearly from 1 through 324. Actually there is no pin 1 on the chip or on the socket. It is intentionally omitted to eliminate any possibility of misalignment. Pin 2 is the leftmost pin in the corner on the top row (near the SBus connector) on the component side.

Two alphanumeric pin identification schemes have been used on the card. In addition to pin numbers, pins can be identified with their relationship to the alphanumeric rows 1 to 18 and A to V. If you already know the signal name and want to know the alpha or numeric pin name, refer to Table 4-8. Also refer to that table if you know the pin name and you wish to find out the signal name.

Figure 4-2 shows the LSC pinout top view. See Figure 4-3 for LSC pinout bottom view.

Table 4-8 shows the LSC signal definitions for the CPGA223 package.

	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
V	324	323	322	321	320	319	318	317	316	315	314	313	312	311	310	309	308	307
U	306	305	304	303	302	301	300	299	298	297	296	295	294	293	292	291	290	289
T	288	287	286	285	284	283	282	281	280	279	278	277	276	275	274	273	272	271
R	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256	255	254	253
P	252	251	250	249											238	237	236	235
N	234	233	232	231											220	219	218	217
M	216	215	214	213											202	201	200	199
L	198	197	196	195											184	183	182	181
K	180	179	178	177											166	165	164	163
J	162	161	160	159					**Top View**						148	147	146	145
H	144	143	142	141											130	129	128	127
G	126	125	124	123											112	111	110	109
F	108	107	106	105											94	93	92	91
E	90	89	88	87											76	75	74	73
D	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55
C	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37
B	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19
A	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	

Figure 4-2 LSC Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
V	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324
U	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306
T	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288
R	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270
P	235	236	237	238											249	250	251	252
N	217	218	219	220											231	232	233	234
M	199	200	201	202											213	214	215	216
L	181	182	183	184											195	196	197	198
K	163	164	165	166					**Bottom View**						177	178	179	180
J	145	146	147	148											159	160	161	162
H	127	128	129	130											141	142	143	144
G	109	110	111	112											123	124	125	126
F	91	92	93	94											105	106	107	108
E	73	74	75	76											87	88	89	90
D	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72
C	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
B	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
A		2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

Figure 4-3 LSC Pinout (Bottom View)

Table 4-8 LSC Signal Pinout Definitions for the CPGA223 Package

Package Pad	Package Pin		Signal
	Alpha	Numeric	
1	D4	58	SB_AB.7
2	C3	39	SB_AB.6
3	B3	21	SB_AB.5
4	A3	3	SB_AB.4
5	D5	59	SB_AB.3
6	C4	40	SB_AB.2
7	B4	22	SB_AB.1
8	A4	4	SB_AB.0
9	C5	41	Unused
10	D6	60	SB_RD
11	B5	23	SB_VIDINIT_
12	C6	42	SB_SIZ.2
13	A5	5	SB_SIZ.1
14	D7	61	SB_SIZ.0
15	B6	24	SB_DB.31
16	C7	43	SB_DB.30
17	A6	6	SB_DB.29
18	D8	62	SB_DB.28
19	B7	7	SB_DB.27
20	C8	44	SB_DB.26
21	A7	7	SB_DB.25
22	D9	63	SB_DB.24
23	B8	26	SB_DB.23
24	C9	45	SB_DB.22
25	B9	27	SB_DB.21
26	B10	28	SB_DB.20
27	A11	11	SB_DB.19
28	C10	46	SB_DB.18
29	B11	29	SB_DB.17

Table 4-8 LSC Signal Pinout Definitions for the CPGA223 Package

Package Pad	Package Pin		Signal
	Alpha	Numeric	
30	D10	64	SB_DB.16
31	A12	12	SB_DB.15
32	C11	47	SB_DB.14
33	B12	30	SB_DB.13
34	D11	65	SB_DB.12
35	A13	13	SB_DB.11
36	C12	48	SB_DB.10
37	B13	31	SB_DB.9
38	D12	66	SB_DB.8
39	A14	14	SB_DB.7
40	C13	49	SB_DB.6
41	B14	32	SB_DB.5
42	C14	50	SB_DB.4
43	D13	67	SB_DB.3
44	A15	15	SB_DB.2
45	B15	33	SB_DB.1
46	D14	68	SB_DB.0
47	C15	51	SB_AS_
48	A16	16	SBUS_CLK
49	B16	34	SB_SEL_
50	D15	69	VA.8
51	C16	52	VA.7
52	C17	53	VA.6
53	C18	54	VA.4
54	E15	87	VA.4
55	D16	70	VA.3
56	D17	71	VA.2
57	D18	72	VA.1
58	F15	105	VA.0
59	F16	106	PDB_7F.7
60	E16	88	PDB_7F.6

Table 4-8 LSC Signal Pinout Definitions for the CPGA223 Package

Package Pad	Package Pin		Signal
	Alpha	Numeric	
61	G15	123	PDB_7F.5
62	E17	89	PDB_7F.4
63	G16	124	PDB_7F.3
64	E18	90	PDB_7F.2
65	H15	141	PDB_7F.1
66	F17	107	PDB_7F.0
67	H16	142	WR_.7
68	F18	108	PDB_6E.7
69	J15	159	PDB_6E.6
70	G17	125	PDB_6E.5
71	J16	160	PDB_6E.4
72	G18	126	PDB_6E.3
73	H17	143	PDB_6E.2
74	H18	144	PDB_6E17
75	K16	178	PDB_6E.0
76	J17	161	WR_.6
77	K15	177	PDB_5D.7
78	K17	179	PDB_5D.6
79	L16	196	PDB_5D.5
80	L17	197	PDB_5D.4
81	L15	195	PDB_5D.3
82	M18	216	PDB_5D.2
83	M16	214	PDB_5D.1
84	M17	215	PDB_5D.0
85	M15	213	WR_.5
86	N18	234	PDB_4C.7
87	N16	232	PDB_4C.6
88	N17	233	PDB_4C.5
89	N15	231	PDB_4C.4
90	P18	252	PDB_4C.3
91	P17	250	PDB_4C.2

Table 4-8 LSC Signal Pinout Definitions for the CPGA223 Package

Package Pad	Package Pin		Signal
	Alpha	Numeric	
92	P16	250	PDB_4C.1
93	R18	270	PDB_4C.0
94	R17	269	WR_.4
95	P15	249	PDB_3B.7
96	R16	268	PDB_3B.6
97	T18	288	PDB_3B.5
98	T17	287	PDB_3B.4
99	R15	267	PDB_3B.3
100	T16	286	PDB_3B.2
101	U16	304	PDB_3B.1
102	V16	322	PDB_3B.0
103	R14	266	WR_.3
104	T15	285	PDB_2A.7
105	U15	303	PDB_2A.7
106	V15	321	PDB_2A.6
107	R13	265	PDB_2A.5
108	T13	283	PDB_2A.4
109	T14	284	PDB_2A.3
110	R12	264	PDB_2A.1
111	U14	302	PDB_2A.0
112	T12	282	WR_.2
113	V14	320	PDB_19.7
114	R11	263	PDB_19.6
115	U13	301	PDB_19.5
116	T11	281	PDB_19.4
117	V13	319	PDB_19.3
118	R10	262	PDB_19.2
119	U12	300	PDB_19.1
120	T10	280	PDB_19.0
121	V12	318	WR_.1
122	U11	317	PDB_08.7

Table 4-8 LSC Signal Pinout Definitions for the CPGA223 Package

Package Pad	Package Pin		Signal
	Alpha	Numeric	
123	V11	299	PDB_08.6
124	T9	279	PDB_08.5
125	U10	298	PDB_08.4
126	R9	261	PDB_08.3
127	U9	297	PDB_08.2
128	T8	278	PDB_08.1
129	U8	296	PDB_08.0
130	R8	260	WR_.0
131	V7	313	OL1.H
132	T7	277	OL1.G
133	U7	295	OL1.F
134	R7	259	OL1.E
135	V6	312	OL1.D
136	T6	276	OL1.C
137	U6	294	OL1.B
138	R6	258	OL1.A
139	V5	311	OL0.H
140	U5	293	OL0.G
141	T5	275	OL0.F
142	V4	310	OL0.E
143	U4	292	OL0.D
144	T4	274	OL0.C
145	R5	257	OL0.B
146	V3	309	TEST_MODE_
147	U3	291	OL0.A
148	R4	256	ID_.2
149	T3	273	ID_.1
151	T1	271	OE0_
152	P4	238	CAS0_
153	R3	255	RAS0_
154	R2	254	WE0_

Table 4-8 LSC Signal Pinout Definitions for the CPGA223 Package

Package Pad	Package Pin		Signal
	Alpha	Numeric	
155	R1	253	PERF_OSC
156	P3	237	WE1_
157	N4	220	SCK1
158	P2	236	SCK0
159	N3	219	BLANK_
160	P1	235	CSYNC_
161	M4	202	CS_DAC_
162	N2	218	B0_SOE1_
163	M3	201	LD
164	N1	217	B0_SOE0_
165	L4	184	CS_ALT_
166	M2	200	B1_SOE1_
167	L3	183	CS_ROM_
168	M1	199	B1_SOE0_
169	K4	166	SB_ACK_.2
170	L2	182	SB_ACK_.1
171	K3	165	SB_ACK_.0
172	L1	181	Unused
173	K2	164	EXT_TXFR_
174	J2	146	SB_RESET_
175	J3	147	DOT_CLK
176	H2	128	SB_AB.23
177	J4	148	ALT_OSC
178	G1	109	SB_AB.22
179	H3	129	MAIN_OSC
180	G2	110	SB_AB.21
181	H4	130	SB_AB.20
182	F1	91	SB_AB.19
183	G3	111	SB_AB.18
184	F2	92	SB_AB.17
185	G4	112	SB_AB.16

Table 4-8 LSC Signal Pinout Definitions for the CPGA223 Package

Package Pad	Package Pin		Signal
	Alpha	Numeric	
186	E1	73	SB_AB.15
187	F3	93	SB_AB.14
188	E2	74	SB_AB.13
189	E3	75	SB_AB.12
190	F4	94	RAS1_
191	D1	55	CAS1_
192	D2	56	OE1_
193	D3	57	SB_AB.11
194	E4	76	SB_AB.10
195	C1	37	SB_AB.9
196	C2	38	SB_AB.8

Legend:

Power (Vdd) Pins:

(alpha) A2, A9, A17, B18, J18, L18, U17, V18, V9, V2, U1, J1, and B1

(numeric) 2, 9, 17, 19, 36, 145, 162, 198, 289, 305, 308, 315, and 324

Ground (Vss) Pins:

(alpha) A8, A10, A18, B17, K18, U18, V17, V10, V8, V1, U2, K1, H1, and B2.

(numeric) 8, 10, 20, 35, 127, 163, 180, 290, 306, 307, 314, 316, and 323

TGX Core 5

This chapter describes the core of the TGX Graphic Accelerator card along with hardware information about the chips that include signal descriptions, handshaking protocol, and timing information. The core consists of the TEC (Transformation Engine and Cursor) block, the FBC (Frame Buffer Controller) block, and memory controller.

Figure 5-1 shows the TGX chip configuration.

The graphic operations accelerated by the TurboGX and TurboGXplus cards are divided between two blocks: TEC and FBC. The TEC block transforms 2-D and 3-D coordinates and provides a programmable hardware cursor. In addition, it controls timing of the video memory and the video signals that drive the monitor. The FBC block renders graphic objects into the video memory.

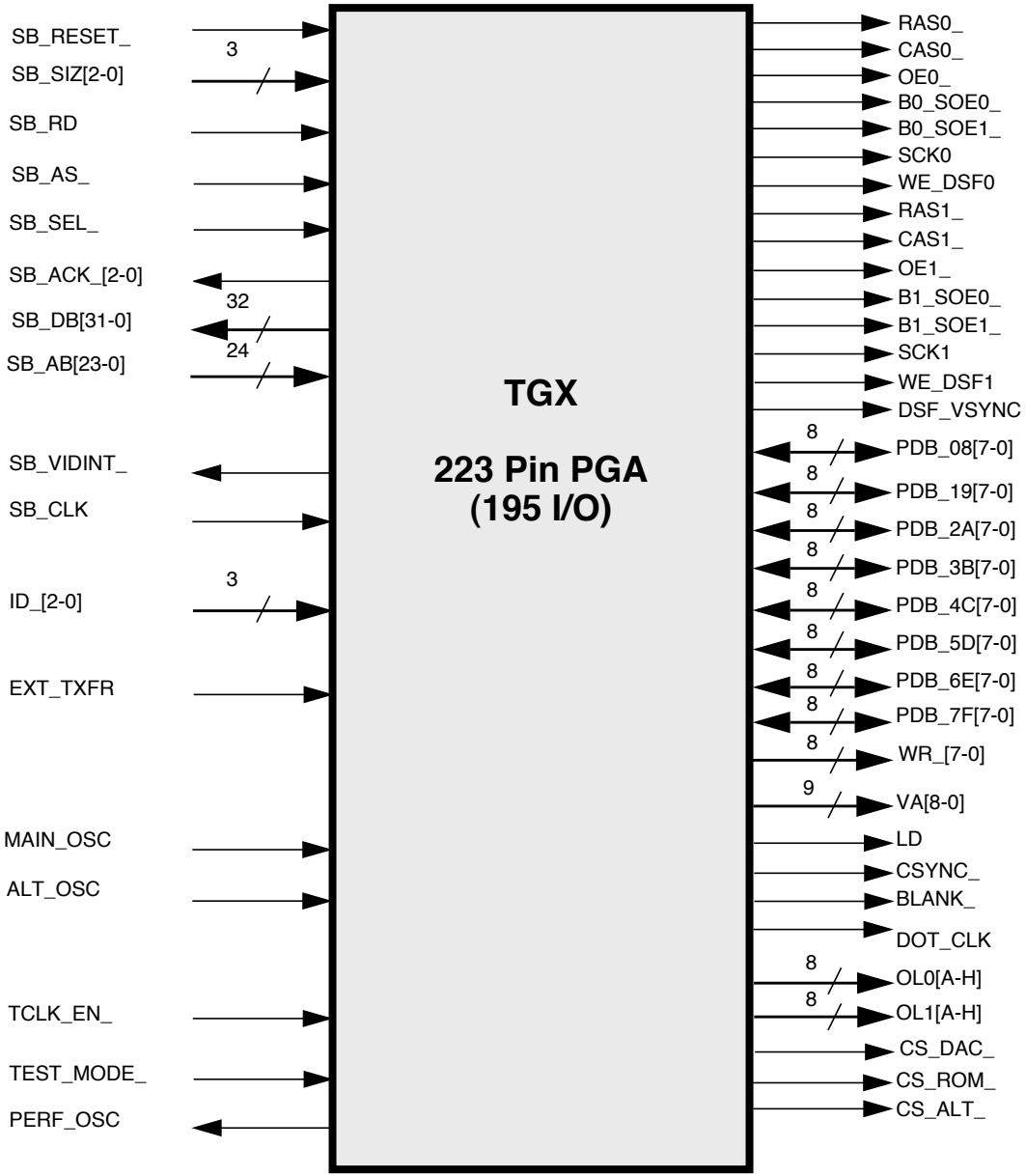


Figure 5-1 TGX Chip Configuration Diagram

5.1 TGXSignal Descriptions

All the signals associated with TGX are described below in detail.

Symbol	Type	Description
SB_RESET	I	SBus Reset. In general, this input causes the TGX to reset to a known state. Various test modes are selected by the state of this input along with the TEST_MODE_ and TCLK_EN_ inputs. See the following section on Testing Methodology for more detail. This pin has a schmidt trigger TTL input and an internal pullup
SB_SIZ[2-0]	I	SBus Size. These inputs tell the TGX the size of the access being made by the SBus. These lines are only used when SB_SEL_ and SB_AS_ are active. The TGX will return an error if the SB_SIZ lines indicate that a BURST cycle has been requested. These pins have internal pullups.
SB_RD	I	SBus Read. This input indicates whether a SBus access is a read (high) or write (low). This pin has an internal pullup.
SB_AS_	I	SB Address Strobe. This input indicates that the SBus address, data, and control signals are valid on the SBus. This pin has an internal pullup.
SB_SEL_	I	SBus Slave Select. This input indicates that the SBus is selecting the TGX for access. This pin has an internal pullup.
SB_ACK_[2-0]	O	SBus Transfer Acknowledge. These outputs indicate the conclusion of a TGX SBus transaction. These lines are normally tristate and get driven actively for only the concluding two cycles of a TGX SBus access. Refer to SBus Specification (P/N 800-4453) for more details.
SB_DB[31-0]	I/O	SBus Data Bus. These pins contain data being transferred between the TGX and the SBus. These pins have internal pullups.

SB_AB[23-0]	I	SBus Address Bus. These pins contain the address of where data is being transferred between the TGX and the SBus. These pins have internal pullups.
SB_VIDINT_	O	SBus Interrupt for VBLANK event. This open-drain output indicates that the TGX is requesting an SBus interrupt to indicate that occurrence of a vertical blanking event.
SB_CLK	I	SBus Clock. This pin provides the basic timing for the TGX's SBus interface logic. It should run in the 16–25 MHz range and should be symmetrical. This pin has Schmidt trigger TTL input and an internal pullup.
ID_[0-2]	I	Identification. These inputs contain the monitor sense code taken from the 13W3 connector. This code shows up in the TGX's CONFIG register within the FBC/FHC address space. These pins have internal pullups. Whenever _MODE_== 0, ID[0] is used as the (uncomplemented) serial scan chain input. ID[1] is used as a high-true scan chain shift enable.
EXT_TXFR	I	External Transfer. When enabled by the EXT_TRANSFER bit in the TGX STRAP register, this input indicates to the TGX that an external memory controller is requesting a transfer cycle. The leading (rising) edge is synchronized and fed to the memory control arbitration logic instead of the transfer signal generated by the TGX timing generation logic. Transfer cycles are given the highest priority and are thus guaranteed service once memory accesses already in progress are concluded. The EXT_TXFR signal needs to be asserted for a minimum time greater than or equal to 3 internal clk periods (64.5ns if the TGX is running internally at 46.48 MHz). The assertion of this signal will

		schedule a split read transfer cycle to start within 8 internal clock periods. Note that the TGX will only provide a Transfer Address of 0 in this mode. The transfer address should be multiplexed in with the VA[8-0] generated by the TGX. This input has an internal pull-up.
MAIN_OSC	I	Main TGX Oscillator. This oscillator input (or a half frequency version of it) is used to clock the core logic of the TGX, transformation engine, and its RAS/CAS/OE memory timing. It can also be selected to provide the basic video timing control and thus be used to generate the DOT_CLK and LD clocks and related synchronous signals. The internal clocking rate can be selected to be either the same as MAIN_OSC (if THC strap[5] == 1) or one half MAIN_OSC (if THC strap[5] == 0). Since the maximum internal clock rate is 50 MHz, MAIN_OSC is restricted to be less than or equal to 100 MHz or 50 MHz depending on the state of THC strap[5]. This signal has a schmidt trigger TTL input with an internal pull-up.
ALT_OSC	I	Alternative Oscillator. This oscillator input (or binary divisions of it) can be selected to provide the basic video timing control and thus be used to generate the DOT_CLK and LD clocks and related synchronous signals. The maximum frequency of ALT_OSC is 117 MHz. This signal has a Schmidt trigger TTL input with an internal pull-up.
TCLK_EN_	I	Test Clock Enable. This input is intended to be utilized on I/C test equipment only. It enables the SBUS_CLK input to be used as the main internal CLK source, allowing the SBus interface to be used synchronously. It also controls the selection of the output PERF_OSC. See the following section on Testing Methodology for more detail. This signal has a schmidt trigger TTL input with an internal pull-up.

TEST_MODE_	I	Test Mode. This input along with the SB_RESET_ and TCLK_EN_determine which test or functional mode the TGX is in. For basic chip functionality, it should be tied high. Refer to the Testing Methodology section for more detail. This signal has a schmidt trigger input and has an internal pull-up.
PERF_OSC	O	Performance Oscillator. This output has different meanings depending upon the state of TEST_MODE_, SB_RESET_, and TCLK_EN_. When selected as the performance oscillator output, a square wave with an approximate frequency of 2.5 MHz should be present. Comparison of this output's frequency with the following chart should help determine the relative timing performance of the device versus simulation at best case, typical and worst case commercial conditions. Refer to the following section on Testing Methodology for more detail.

Table 5-1 Timing Performance of the Device(testing in progress - TBD)

Condition	Frequency	Period
Best case	-	-
Typical	-	-
Worst case	-	-

RAS0,_CAS0_, OE0	O	Bank 0 VRAM control. In single buffered H/W applications, these outputs are intended to drive the VRAM control inputs. In double buffered H/W applications, these outputs should drive just BANK 0 VRAM control inputs.
B0_SOE0_ , B0_SOE1_	O	Bank 0 VRAM Serial Data Output Enable 0. In hardware applications with a 4-pixel wide DAC B0_SOE0_ and B0_SOE1_ alternate for each shift clock to multiplex 8 pixels down into the 4-pixel DAC input. In hardware applications with an 8-pixel wide DAC, B0_SOE0_ and B0_SOE1_ are both low continuously. Single buffered hardware

		applications use only B0_SOE0_ and B0_SOE1_. These outputs are synchronous within the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
SCK0	O	Bank 0 serial shift clock. In single buffered H/W applications, this output is intended to drive the VRAM shift clock inputs. In double buffered H/W applications, this output should drive just BANK 0 VRAM shift clock inputs. This output is synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
WE_DSF0	O	Bank 0 Write Enable or DSF. When the TGX is used in a compatibility mode (THC strap [18] == 0) with an LSC/LAF on a Duplo/Quadro configuration, this output will be always "low" so as to enable all writes through the external "OR" gates. When the TGX is in alternate DSF mode (THC strap [18] == 1), this pin is the TGX's DSF output pin for driving the bank 0 VRAM DSF input pins in a one or two bank system.
RAS1_, CAS1_, OE1	O	Bank 1 VRAM control. In single buffered H/W applications, these outputs are not used. In double buffered H/W applications, these outputs should drive just BANK 1 VRAM control inputs.
B1_SOE0_, B1_SOE1_	O	Bank 1 VRAM Serial Output Enable 0. This output as well as B1_SOE1_ are the serial output enables for the 2nd bank in double buffer hardware applications. B1_SOE0_ and B1_SOE1_ alternate on each shift clock when bank 1 is being displayed. They remain high when bank 0 is displayed.
SCK1	O	Bank 0 serial shift clock. In single buffered H/W applications, this output is not used. In double buffered H/W applications, this output should drive just BANK 1 VRAM shift clock inputs. This

output is synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.

WE_DSF1 O Bank 1 Write Enable or DSF. When the TGX is used in a compatibility mode (THC strap [18] == 0) [with an LSC/LAF on a Duplo/Quadro configuration,] this output will be always "low" so as to enable all writes through the external "OR" gates.

When the TGX is in alternate DSF mode (THC strap [18] == 1), this pin is the TGX's DSF output pin for driving the bank 1 VRAM DSF input pins in a two bank system.

When in a 1 bank system, this output will always be "low".

DSF_VSYNC O VSync or DSF. When the TGX is used in a compatibility mode (THC strap [18] == 0) with an LSC/LAF, this pin is the TGX's DSF output for driving all bank's VRAM DSF input pins.

When the TGX is in alternate DSF mode (THC strap [18] == 1) this pin is the TGX's VSync_ output pin. When asserted, the TGX video is in vertical Sync.

PDB_xx[7:0] I/O Pixel data bus. These pins are bidirectional data lines that transfer data to and from the VRAM memory. Table 5-2 shows how the data lines should be connected. In this table, the pixel 0 is the leftmost pixel and pixel 7 is the rightmost pixel. These pins have internal pullups.

Table 5-2 Data Lines Connections for Pixel Data Bus

Data	**Bank 0**	**Bank 1 (only for double buffer board**
PDB_08	Pixel 0	Pixel 0
PDB_19	Pixel 1	Pixel 1
PDB_2A	Pixel 2	Pixel 2

Data	Bank 0	Bank 1 (only for double buffer board
PDB_3B	Pixel 3	Pixel 3
PDB_4C	Pixel 4	Pixel 4
PDB_5D	Pixel 5	Pixel 5
PDB_6E	Pixel 6	Pixel 6
PDB_7F	Pixel 7	Pixel 7

WR_[7-0] O Write Enable. These outputs are used to enable individual pixels during VRAM write cycles. All WR_ signals are driven low when the row address is on the address bus for loading the plane mask into the video RAMs.

VA[8-0] O VRAM address. These outputs can be used to drive the multiplexed VRAM address inputs directly. The linear address bits that appear on the VA output bus is a function of the memory control operation and the type of VRAM utilized (indicated in the THC address space's STRAP register). The usage of the VA lines is described in the following table.

Table 5-3 VA Lines Usage

Control Operation	128K x 8	256K x 4
normal RAS	LA[19-11]	LA[20-12]
normal CAS	LA[11-4], B	LA[11-4], B
transfer RAS	TA[8-0]	TA[8-0]
transfer CAS	0s	0s

Legend:

LA[xx] refers to linear address bits.

TA[xx] refers to the transfer address counter.

B refers to internally generated interleave select bit.

LD O Load clock. This output is derived from the oscillator input selected to generate the DOT_CLK output. This output can be a divide-by-4 or a

		divide-by-8 of the DOT_CLK frequency depending on the DAC_MUX setting in the THC address space STRAP register.
CSYNC_	O	Composite Sync. This output is the combined sync signal for use by the monitor. This output is synchronous with the oscillator input (MAIN OSC or ALT_OSC) selected for video timing generation.
BLANK_	O	Blank. This output is the blanking signal for the video DACs. This output is synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
DOT_CLK	O	Video dot clock. This output can be selected via the THC address space STRAP register to reflect either the MAIN_OSC or ALT_OSC input.
OL0A-H]	O	Overlay planes. These outputs are for plane 0 of the hardware cursor. Groups of four planes use OL0[A-H]. Bit A is the leftmost pixel. These outputs are synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
CS_DAC_	O	DAC chip select. This output is asserted low when the TGX detects an SBus access intended for the DAC.
CS_ROM_	O	ROM chip select. This output is asserted low when the TGX detects an SBus access intended for the DAC.
CS_ALT_	O	Alternate chip select. This output is asserted low when the TGX detects an SBus access intended for an external device accessed through the alternate device address space.

5.2 Testing Methodology

Table 5-4 SB_RESET_ in TEST_MODE_

TEST_MODE_	SB_RESET_	Characteristics
0	0	Enable scan chain shifting, force main_osc==clk2x==clk, force_main_osc==ld_clk2x==ld_clk, select scan output on PERF_OSC, reset (clear) THC STRAP register, ID_ [0]=scan input, ID_ [1]=scan enable
0	1	Tristate all outputs, force main_osc==clk2x==2*clk, force main_osc==ld_clk2x==2*ld_clk, select Param. Nand tree on PERF_OSC, reset (clear) THC STRAP register.
1	0	known state, Select Param. Nand tree on PERF_OSC_.
1	1	Normal functional mode, select performance osc on PERF_OSC.

Note – clk, clk2x, ld_clk2x, and ld_clk are TGX internal signals.

When the TEST_MODE_==1, SB_RESET_ is assumed to be synchronous to SB_CLK. When TEST_MODE_==0, SB_RESET_ is assumed synchronous with MAIN_OSC. This pin has a Schmidt trigger TTL input and an internal pullup.The testing methodology for the TGX utilizes three basic approaches: partial scan, parallel functional access, and special test modes for achieving the targeted fault coverage (>95%) requirement. The approaches used for each of the major modules comprising the TGX are:

CLOCK_GEN: Fault coverage via normal functional patterns

FBC_CORE: Fault coverage via normal functional patterns and partial scan (90%+ of flip-flops scanned).

TEC_CORE Fault coverage via normal functional patterns and scan only for signals provided to the FBC_CORE.

MCTRL_LOGIC	Partial scan (50%+ of flip-flops scanned)
SBUS_LOGIC	Partial scan (90%+ of flip-flops scanned)

Partial (as opposed to full scan) has been used throughout the design due to the usage of some negative edge, 2x speed flip-flops, as well as the need to reduce the design size. The design also contains numerous latch-based storage elements. These elements are maintained in a transparent mode while the design is in scan test mode. Non-scanned flip-flops are either prevented from changing state while shifting in/out scan patterns or are prevented (or isolated) from affecting scannable circuitry while the TGX is in scan test mode.

One type of scan employed by the TGX is a single scan chain with a common single-edged clock (same clock that is used in functional mode) with a global scan-shift enable pin/signal.

The scannable portions of the chip are to be tested via functional patterns and ATPG patterns. The non-scannable portions of the chip are to be tested via functional patterns only.

Note, the design will use ~80K parallel test vectors in addition to the ATPG-generated serial scan vectors. The scan chain is approximately 1134 elements long.

Also included in the design is a free-running internally-generated oscillator (PERF_OSC) that is accessible at a pin on the chip. The period of this oscillator should directly reflect the AC performance characteristics of the TGX's core logic. Table 5-5 shows the dc parameters. Table 5-6 shows the pin loading assumptions.

Table 5-5 DC Parameters

Parameter	Signals	Conditions	Min	Max	Unit
Voh	PERF_OSC	Ioh =-1mA	2.4		V
Voh	LD, CS_xxx CSYNC_,BLANK_ OL0[A-H], OL1[A-H], WEx_	Ioh = -2mA	2.4		V
Voh	PDB, SB_DB, WR_[7:0], DOT_CLK,	Ioh = -4mA	2.4		V
			2.4		V

Parameter	Signals	Conditions	Min	Max	Unit
	Bx_SOEy_				
Voh	RASx_, CASx_, OEx_,SCKx, VA	Ioh = -6mA	2.4		V
Voh	SB_ACK_[2:0]	Ioh = -8mA	2.4		V
Voh	PERF_OSC	Iol = 1mA	0.8		V
Voh	LD, TXD, CS_xxx, CSYNC, BLANK_ OL0[A-H], OL1[A-H], WEx_	Iol = 2mA	0.8		V
Vol	PDB, SB_DB, WR_[7:0], Bx_SOEy_, SB_VIDINT_*,DOT_CLK	Iol - 4mA	0.8		V
Vol	RASx_, CASx_, OEx_, SCKx, VA	Iol = -6mA	0.8		V
Vol	SB_ACK_[2:0]	Iol= - 8mA	0.8		V
Vih				0.8	V
Vil			2.4		V
Li	All inputs	0 < VI < Vcc	50	100	uA
Ri	All inputs	input pullup	50K	100K	Ohms
Vcc			4.75	5.25	V
Icc				~300	mA
Ci	All inputs			12	pF

*Open drain output

Table 5-6 Pin Loading Assumptions

Output	Loading
PERF_OSC	10pF
VA[8:0]	100pF
RASx_	120 pF
CASx_	120 pF
OEx_	120 pF
B0_SOEx_	60 pF

Output	Loading
B1_SOEx_	60 pF
SCKx	120 pF
WR_[7:0]	40 pF
WEx_	50 pF
SB_DB[23:0]	160 pF
SB_ACK[2:0]	120 pF
PDB_xx[7:0]	30 pF
SB_VIDINT_	120 pF
CSYNC_	15 pF
BLANK_	15 pF
LD	15 pF
DOT_CLK	20 pF
OL0[A-H]	15 pF
Ol1[A-H]	15 pF
CS_XXX_	25 pF
SB_RESET	120 pF

5.3 TGXPackaging

The TGX is in a 223-pin package in a 18 x 18 grid of pins numbered linearly from 1 through 324. Actually there is no pin 1 on the chip or on the socket. It is intentionally omitted to eliminate any possibility of misalignment. Pin 2 is the leftmost pin in the corner on the top row (near the SBus connector) on the component side.

Two alphanumeric pin identification schemes have been used on the card. In addition to pin numbers, pins can be identified with their relationship to the alphnumeric rows 1 to 18 and A to V. If you already know the signal name and want to know the alpha or numeric pin name, refer to Table 5-7. Also refer to that table if you know the pin name and you wish to find out the signal name.

Figure 5-2 shows the TGX pinout top view. See Figure 5-3 for TGX pinout bottom view.

Table 5-7 shows the TGX signal definitions for the CPGA223 package.

	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
V	324	323	322	321	320	319	318	317	316	315	314	313	312	311	310	309	308	307
U	306	305	304	303	302	301	300	299	298	297	296	295	294	293	292	291	290	289
T	288	287	286	285	284	283	282	281	280	279	278	277	276	275	274	273	272	271
R	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256	255	254	253
P	252	251	250	249											238	237	236	235
N	234	233	232	231											220	219	218	217
M	216	215	214	213											202	201	200	199
L	198	197	196	195											184	183	182	181
K	180	179	178	177											166	165	164	163
J	162	161	160	159				**Top View**							148	147	146	145
H	144	143	142	141											130	129	128	127
G	126	125	124	123											112	111	110	109
F	108	107	106	105											94	93	92	91
E	90	89	88	87											76	75	74	73
D	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55
C	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37
B	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19
A	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	

Figure 5-2 TGX Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
V	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324
U	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306
T	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288
R	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270
P	235	236	237	238											249	250	251	252
N	217	218	219	220											231	232	233	234
M	199	200	201	202											213	214	215	216
L	181	182	183	184											195	196	197	198
K	163	164	165	166				**Bottom View**							177	178	179	180
J	145	146	147	148											159	160	161	162
H	127	128	129	130											141	142	143	144
G	109	110	111	112											123	124	125	126
F	91	92	93	94											105	106	107	108
E	73	74	75	76											87	88	89	90
D	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72
C	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
B	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
A		2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

Figure 5-3 TGX Pinout (Bottom View)

Table 5-7 TGX Signal Pinout Definitions for the CPGA223 Package

Package Pad	Package Pin		Signal
	Alpha	Numeric	
1	D4	58	SB_AB.7
2	C3	39	SB_AB.6
3	B3	21	SB_AB.5
4	A3	3	SB_AB.4
5	D5	59	SB_AB.3
6	C4	40	SB_AB.2
7	B4	22	SB_AB.1
8	A4	4	SB_AB.0
9	C5	41	Unused
10	D6	60	SB_RD
11	B5	23	SB_VIDINIT_
12	C6	42	SB_SIZ.2
13	A5	5	SB_SIZ.1
14	D7	61	SB_SIZ.0
15	B6	24	SB_DB.31
16	C7	43	SB_DB.30
17	A6	6	SB_DB.29
18	D8	62	SB_DB.28
19	B7	7	SB_DB.27
20	C8	44	SB_DB.26
21	A7	7	SB_DB.25
22	D9	63	SB_DB.24
23	B8	26	SB_DB.23
24	C9	45	SB_DB.22
25	B9	27	SB_DB.21
26	B10	28	SB_DB.20
27	A11	11	SB_DB.19
28	C10	46	SB_DB.18
29	B11	29	SB_DB.17
30	D10	64	SB_DB.16

Package Pad	Package Pin		Signal
	Alpha	Numeric	
31	A12	12	SB_DB.15
32	C11	47	SB_DB.14
33	B12	30	SB_DB.13
34	D11	65	SB_DB.12
35	A13	13	SB_DB.11
36	C12	48	SB_DB.10
37	B13	31	SB_DB.9
38	D12	66	SB_DB.8
39	A14	14	SB_DB.7
40	C13	49	SB_DB.6
41	B14	32	SB_DB.5
42	C14	50	SB_DB.4
43	D13	67	SB_DB.3
44	A15	15	SB_DB.2
45	B15	33	SB_DB.1
46	D14	68	SB_DB.0
47	C15	51	SB_AS_
48	A16	16	SBUS_CLK
49	B16	34	SB_SEL_
50	D15	69	VA.8
51	C16	52	VA.7
52	C17	53	VA.6
53	C18	54	VA.4
54	E15	87	VA.4
55	D16	70	VA.3
56	D17	71	VA.2
57	D18	72	VA.1
58	F15	105	VA.0
59	F16	106	PDB_7F.7
60	E16	88	PDB_7F.6
61	G15	123	PDB_7F.5
62	E17	89	PDB_7F.4

Package Pad	Package Pin		Signal
	Alpha	Numeric	
63	G16	124	PDB_7F.3
64	E18	90	PDB_7F.2
65	H15	141	PDB_7F.1
66	F17	107	PDB_7F.0
67	H16	142	WR_.7
68	F18	108	PDB_6E.7
69	J15	159	PDB_6E.6
70	G17	125	PDB_6E.5
71	J16	160	PDB_6E.4
72	G18	126	PDB_6E.3
73	H17	143	PDB_6E.2
74	H18	144	PDB_6E17
75	K16	178	PDB_6E.0
76	J17	161	WR_.6
77	K15	177	PDB_5D.7
78	K17	179	PDB_5D.6
79	L16	196	PDB_5D.5
80	L17	197	PDB_5D.4
81	L15	195	PDB_5D.3
82	M18	216	PDB_5D.2
83	M16	214	PDB_5D.1
84	M17	215	PDB_5D.0
85	M15	213	WR_.5
86	N18	234	PDB_4C.7
87	N16	232	PDB_4C.6
88	N17	233	PDB_4C.5
89	N15	231	PDB_4C.4
90	P18	252	PDB_4C.3
91	P17	250	PDB_4C.2
92	P16	250	PDB_4C.1
93	R18	270	PDB_4C.0
94	R17	269	WR_.4

Package Pad	Package Pin		Signal
	Alpha	Numeric	
95	P15	249	PDB_3B.7
96	R16	268	PDB_3B.6
97	T18	288	PDB_3B.5
98	T17	287	PDB_3B.4
99	R15	267	PDB_3B.3
100	T16	286	PDB_3B.2
101	U16	304	PDB_3B.1
102	V16	322	PDB_3B.0
103	R14	266	WR_.3
104	T15	285	PDB_2A.7
105	U15	303	PDB_2A.7
106	V15	321	PDB_2A.6
107	R13	265	PDB_2A.5
108	T13	283	PDB_2A.4
109	T14	284	PDB_2A.3
110	R12	264	PDB_2A.1
111	U14	302	PDB_2A.0
112	T12	282	WR_.2
113	V14	320	PDB_19.7
114	R11	263	PDB_19.6
115	U13	301	PDB_19.5
116	T11	281	PDB_19.4
117	V13	319	PDB_19.3
118	R10	262	PDB_19.2
119	U12	300	PDB_19.1
120	T10	280	PDB_19.0
121	V12	318	WR_.1
122	U11	317	PDB_08.7
123	V11	299	PDB_08.6
124	T9	279	PDB_08.5
125	U10	298	PDB_08.4
126	R9	261	PDB_08.3

Package Pad	Package Pin		Signal
	Alpha	Numeric	
127	U9	297	PDB_08.2
128	T8	278	PDB_08.1
129	U8	296	PDB_08.0
130	R8	260	WR_.0
131	V7	313	OL1.H
132	T7	277	OL1.G
133	U7	295	OL1.F
134	R7	259	OL1.E
135	V6	312	OL1.D
136	T6	276	OL1.C
137	U6	294	OL1.B
138	R6	258	OL1.A
139	V5	311	OL0.H
140	U5	293	OL0.G
141	T5	275	OL0.F
142	V4	310	OL0.E
143	U4	292	OL0.D
144	T4	274	OL0.C
145	R5	257	OL0.B
146	V3	309	TEST_MODE_
147	U3	291	OL0.A
148	R4	256	ID_.2
149	T3	273	ID_.1
151	T1	271	OE0_
152	P4	238	CAS0_
153	R3	255	RAS0_
154	R2	254	WE0_
155	R1	253	PERF_OSC
156	P3	237	WE1_
157	N4	220	SCK1
158	P2	236	SCK0
159	N3	219	BLANK_

Package Pad	Package Pin		Signal
	Alpha	Numeric	
160	P1	235	CSYNC_
161	M4	202	CS_DAC_
162	N2	218	B0_SOE1_
163	M3	201	LD
164	N1	217	B0_SOE0_
165	L4	184	CS_ALT_
166	M2	200	B1_SOE1_
167	L3	183	CS_ROM_
168	M1	199	B1_SOE0_
169	K4	166	SB_ACK_.2
170	L2	182	SB_ACK_.1
171	K3	165	SB_ACK_.0
172	L1	181	Unused
173	K2	164	EXT_TXFR_
174	J2	146	SB_RESET_
175	J3	147	DOT_CLK
176	H2	128	SB_AB.23
177	J4	148	ALT_OSC
178	G1	109	SB_AB.22
179	H3	129	MAIN_OSC
180	G2	110	SB_AB.21
181	H4	130	SB_AB.20
182	F1	91	SB_AB.19
183	G3	111	SB_AB.18
184	F2	92	SB_AB.17
185	G4	112	SB_AB.16
186	E1	73	SB_AB.15
187	F3	93	SB_AB.14
188	E2	74	SB_AB.13
189	E3	75	SB_AB.12
190	F4	94	RAS1_
191	D1	55	CAS1_

Package Pad	Package Pin		Signal
	Alpha	Numeric	
192	D2	56	OE1_
193	D3	57	SB_AB.11
194	E4	76	SB_AB.10
195	C1	37	SB_AB.9
196	C2	38	SB_AB.8

Legend:

Power (Vdd) Pins:

(alpha) A2, A9, A17, B18, J18, L18, U17, V18, V9, V2, U1, J1, and B1

(numeric) 2, 9, 17, 19, 36, 145, 162, 198, 289, 305, 308, 315, and 324

Ground (Vss) Pins:

(alpha) A8, A10, A18, B17, K18, U18, V17, V10, V8, V1, U2, K1, H1, and B2.

(numeric) 8, 10, 20, 35, 127, 163, 180, 290, 306, 307, 314, 316, and 323

Video Memory 6

This chapter provides a functional description of the video memory of the GX, GXplus,TurboGXplus, and TurboGX cards. It covers video memory architecture, data side timing, and video side timing. The first part of this chapter contains video memory information on the GX and GXplus cards. The second part of this chapter contains video memory information on the TurboGX card. If you are interested in TurboGX and TurboGXplus video memory only, refer to section 6.5.

6.1 LSC Memory Architecture

The LSC chip supports four different memory configurations:

- 1 megabyte with eight 128k x 8 100 nS VRAMs
- 2 megabytes high resolution single buffer with 16 256k x 4 100 nS VRAMs
- 2 megabytes low resolution double buffer or high resolution single buffer with 16 128k x 8 100 nS VRAMs
- 4 megabytes high resolution double buffer with 32 256k x 4 100 nS VRAMs

Refer to Chapter 7 for block diagrams of memory architecture for a particular board.

6.1.1 Data Side Architecture

The video address (VA<8..0>) is common to all memory chips regardless of configuration. Configurations with more than 16 memory chips need external buffering on the (VA<8..0>) bus. The address is multiplexed in the form of a VRAM row address and column address. The VRAM rows do not correspond to scan lines on the screen. There is a new row address every 2048 pixels for 128k x 8 VRAMs and every 4096 pixels for configurations with 256k x 4 VRAMs. The VRAMs have a fast page mode which allows faster accesses if the row address does not change. The VRAMs remember the row address so subsequent addresses anywhere within the current row only require a column address and a column address strobe (CAS0* for bank 0 and CAS1* for bank 1). Fast page mode reads are double accesses which take a total of three cycles (129 nS). A non-page mode read takes 6 cycles (258 nS). Dumb Frame Buffer (DFB) writes are single writes that take only two cycles (86 nS) for fast page mode and five cycles (215 nS) for non-page mode. FBC writes are double writes that take three cycles (129 nS). In all cases, changing the row address adds a three cycle (129 nS) penalty to the access time.

6.1.2 Video Side Architecture

Note that the serial input to the Palette DAC is 32 bits wide. Therefore, the serial output data from the Video Memory to the Palette DAC must be interleaved 2 to 1. During the SOE0* output enable signal, bits 0 through 7 of pixels 0 through 3 are transferred to the Palette DAC on signal lines PA<7.. 0> through PD<7.. 0>, respectively. Then the SOE1* signal enables pixels 4 through 7 on the same signal lines.

6.2 Data Side Timing

and Table 6-2 show the most important timing requirements for VRAM used with the LSC chip. The parameters are illustrated in Figure 6-1, Figure 6-2, and Figure 6-6.

6.2.1 Read Cycle

All read cycles are actually double accesses where the first one is an even address location and the second is an odd location. The first read is likely to be a random read (Figure 5-1) where both a row and a column address are necessary. Subsequent accesses to the same VRAM row only require a new column address (Fast Page Mode).

The random read starts with a RAS* precharge high pulse lasting two clocks (86 nS). The falling edge of RAS* latches in the row address from the 9-bit VRAM address bus VA<8-0>. FBC_DOE_ is the Pixel Data Bus PDB_xx output enable inside the LSC chip. FBC_DOE_ and the write enables WRx_ are low at the falling edge of RAS* to update the pixel plane mask inside the VRAM. The plane mask is only used for writing to the VRAM, but it is simpler to update it for every random access.

The falling edge of CAS* latches in the column address. CAS* low and OE* low enable the VRAM data outputs onto the PDB_xx bus. The read data will be valid after tRAC, tAA, tCAC, and tOEA are satisfied. Typically, the data will be valid 30 nS after the falling edge of CAS* at the VRAM assuming tCAC = 30 nS. DACK0 and DACK1 are the two data latch enable signals inside the LSC chip. When the DAC signals are high, the PDB_xx latches are open. The DACK signals do not come out of the chip, but their edges line up with the CAS* edges. This means that the read data must be valid at the LSC chip before the rising edge of CAS* at the LSC chip.

6.2.2 Write Cycle

The LSC has two types of write cycles. Figure 6-2 shows an “FBC” write cycle which is a double access. The acronym FBC is leftover from the original GX card where the Frame Buffer Controller (FBC) was a separate chip. The FBC accesses include all drawing operations, fonts, and BLITs.

The random write cycle starts with a RAS* precharge high pulse just like the random read. The falling edge of RAS* latches in the row address and plane mask. The plane mask determines which bits of the pixel will be written. The LSC chip output enable FBC_DOE is active for all but the first clock cycle of the random write.

The falling edge of CAS* latches in the column address. The LSC uses a late write or OE controlled write as opposed to an early write. This means that the write data is not latched into the VRAM until the falling edge of the write enable WRx_. The write lines WR<7-0>_ determine which of the 8 pixels are actually written to the VRAM. Any combination of pixels can be enabled using a pixel mask register inside the LSC.

FBC writes are double accesses so a random write will always be followed by a fast page write. The LSC deals with 16 pixels at a time so it writes the first 8 pixels to an even column address with the first CASx pulse and then writes the second 8 pixels to the odd column address. Both writes may be fast page writes if the previous access had the same row address. A fast page write access is shown in Figure 6-3.

A dead state is required to change the direction of the pixel data bus from a read to a write. Figure 6-3 shows that both the VRAM output enable OEx_ and the LSC output enable FBC_DOE_ are inactive during the dead state. A dead state is not required when going from write to read because all read cycles have a half clock of dead time built into the beginning of the cycle.

The second type of write cycle is the Dumb Frame Buffer (DFB) write. The DFB access mode provides the host computer direct access to the frame buffer memory through the SBus and LSC chip. The SBus interface is 32 bits (4 pixels) wide so a double CAS* FBC write cycle would have been wasteful for DFB writes. To avoid that, a single CAS* cycle is used. CAS* stays low for 1.5 clock cycles instead of 1 clock cycle for FBC accesses.

6.2.3 *Refresh*

Video RAM is a dynamic memory with tiny capacitors as storage cells which must be recharged periodically. The 1 Meg VRAMs supported by LSC must be refreshed entirely every 8 mS. LSC does this by refreshing one of the 512 rows every 15.6 mS. The refresh cycle takes five clocks (215 nS) and is a CAS before RAS style which uses a row counter inside each VRAM to determine the row to be refreshed. Refresh overwrites the row address stored in the VRAM so the first access after a refresh is forced to be a non-page mode access.

6.2.4 *Video Transfer*

Video RAMs are dual ported with a serial port as well as a random access port. There is a serial access memory that is loaded in parallel with one row of data then shifted out while the LSC is using the random port. The parallel loading is the real time read transfer cycle. The falling edge of OE* while RAS* is high, signals the start of the transfer cycle. The transfer row address is latched into the VRAM by the falling edge of RAS*. When CAS* drops, it latches in the starting address for the shifter which is always 0 in the LSC design. The trailing edge of OE* is synchronous with the video shift clock instead of RAS* and CAS* edges. The end of the OE* low pulse triggers the actual data transfer from the main memory to the serial access memory.

The video transfer occurs every 2048 pixels in configurations with 128k x 8 VRAMs and every 4096 pixels in 256k x 4 VRAM configurations.

Figure 6-6 also shows the serial port read timing. The shift clock SCKx advances the serial shifter in all the VRAMs at once. The serial output enables BxSOE0_ and BxSOE1_ alternate to enable four pixels at a time onto the pixel bus Px<7-0>. The DAC load LD clocks in the pixel data and overlay data on the rising edge. The overlay data comes directly from the LSC chip and is used for the hardware cursor.

The following figures describe data side timing diagrams:

Figure 6-1 VRAM Read cycle (for both FBC and DFB Reads)

Figure 6-2 FBC to VRAM Write Cycle (OE_controlled Write)

Figure 6-3 Any Read Followed by Fast Page Write

Figure 6-4 DFB to VRAM Random Write, Fast Page Write, Idle (OE_Controlled Writes)

Figure 6-5 CAS_Before RAS_ Refresh

Figure 6-6 Real Time Read Transfer and Serial Read (with 4 pixel wide DAC)

Figure 6-7 Fast Copy From Buffer 1 to Buffer 0 (for double-buffered card)

Figure 6-8 Real Time Read Transfer and Serial Read with 8 pixel wide DAC

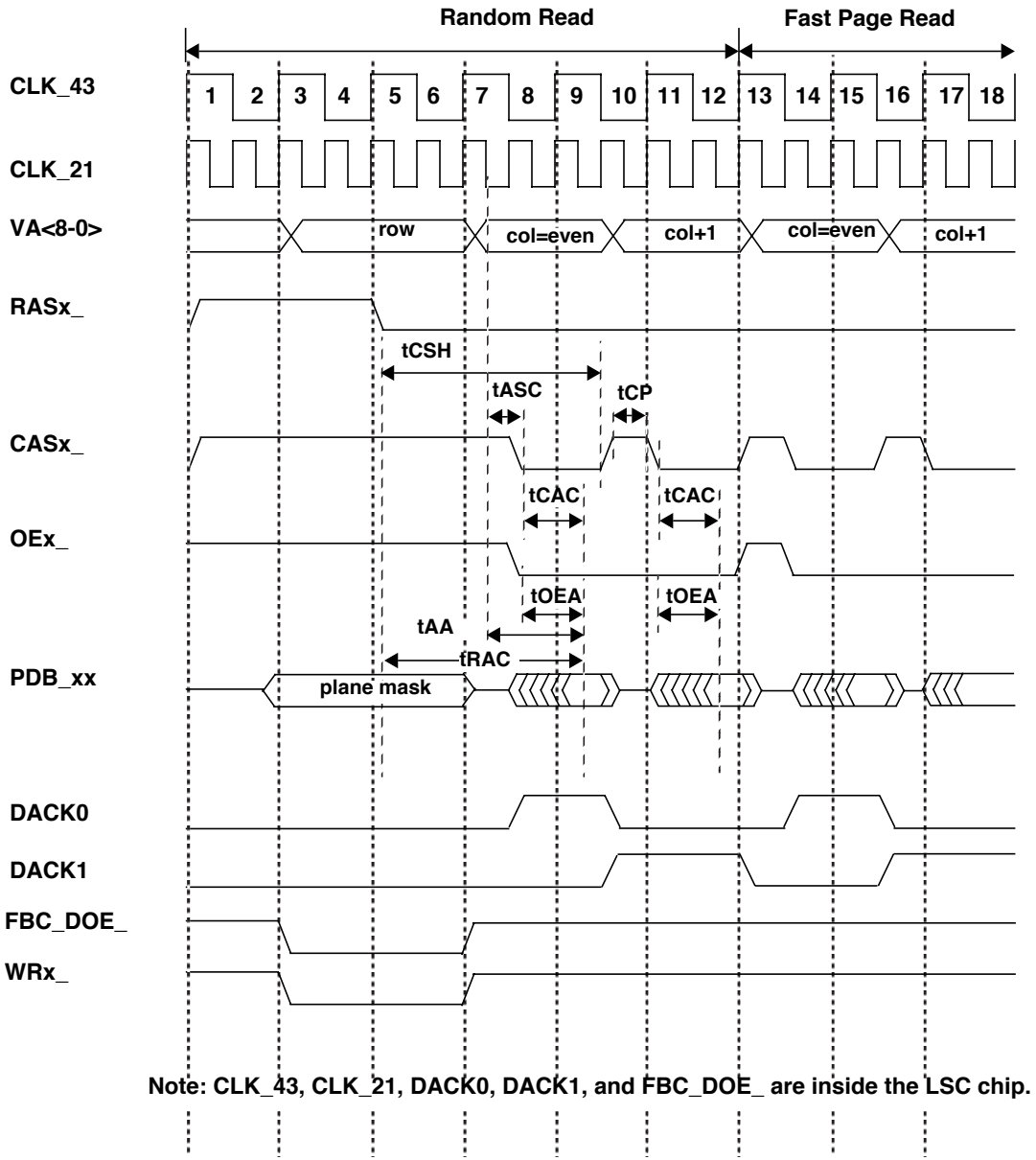


Figure 6-1 VRAM Random Read Cycle (for Both FBC and DFB Reads)

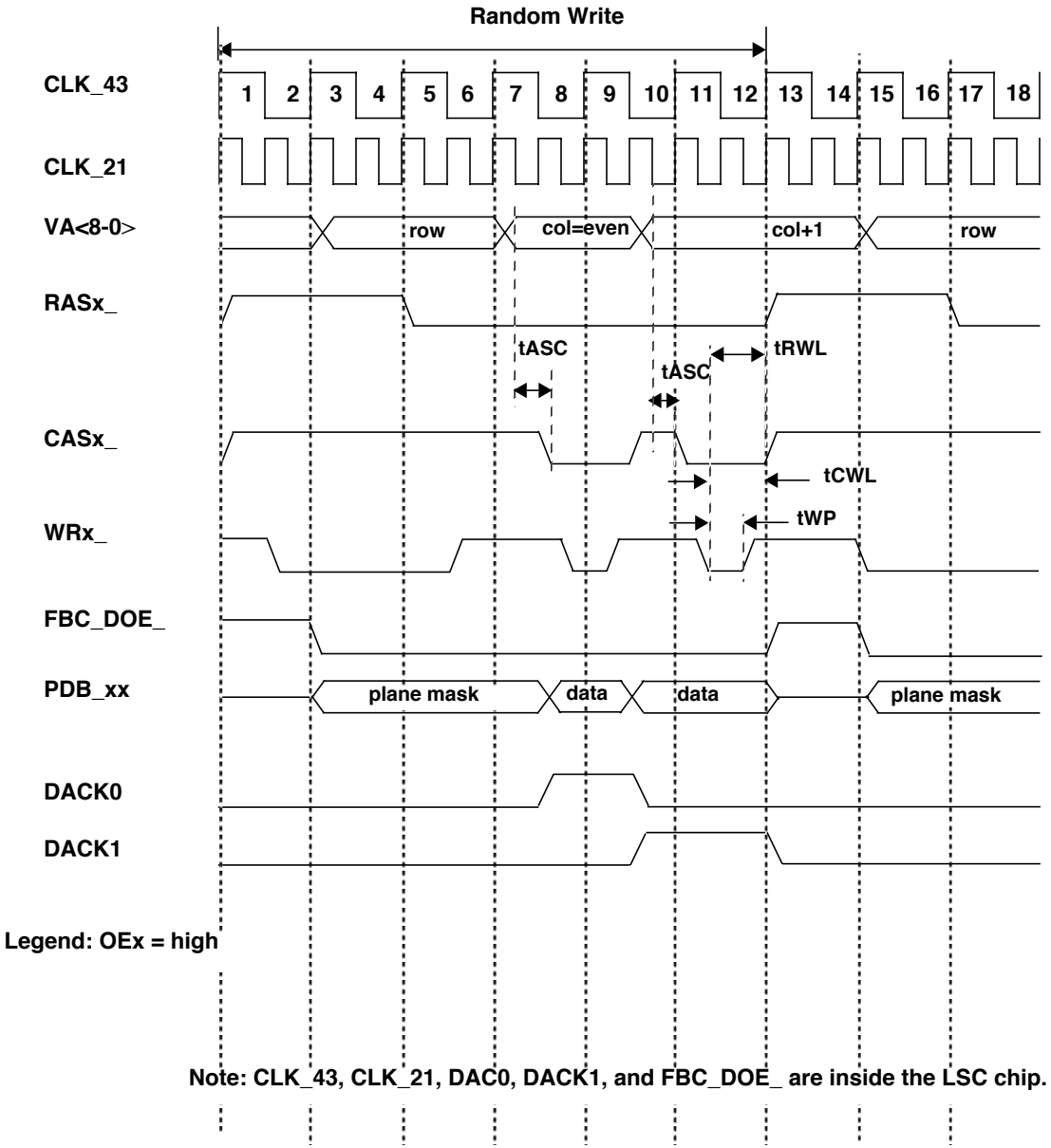


Figure 6-2 FBC to VRAM Write Cycle (OE_Controlled Write)

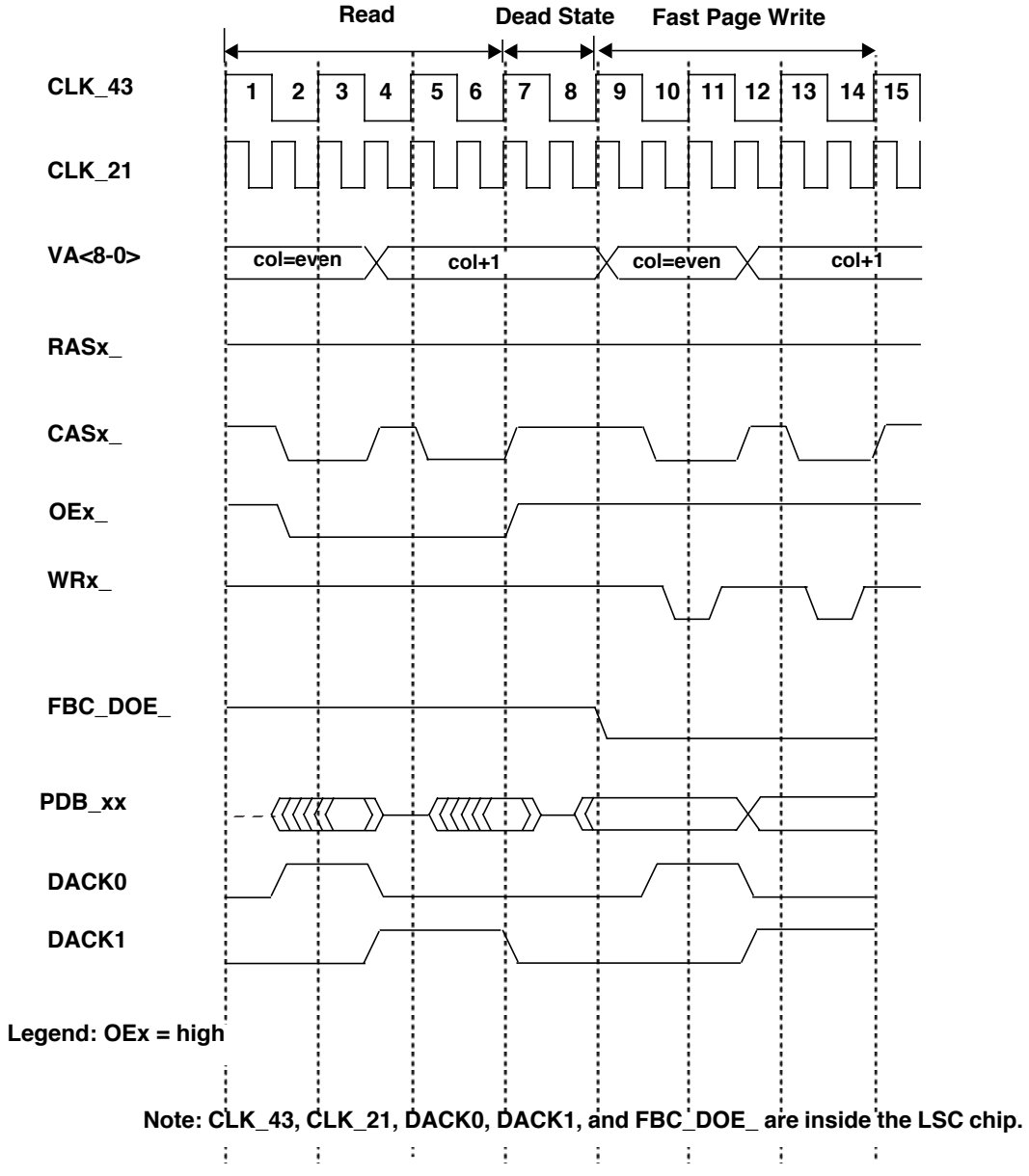


Figure 6-3 Any Read Followed by Fast Page Write

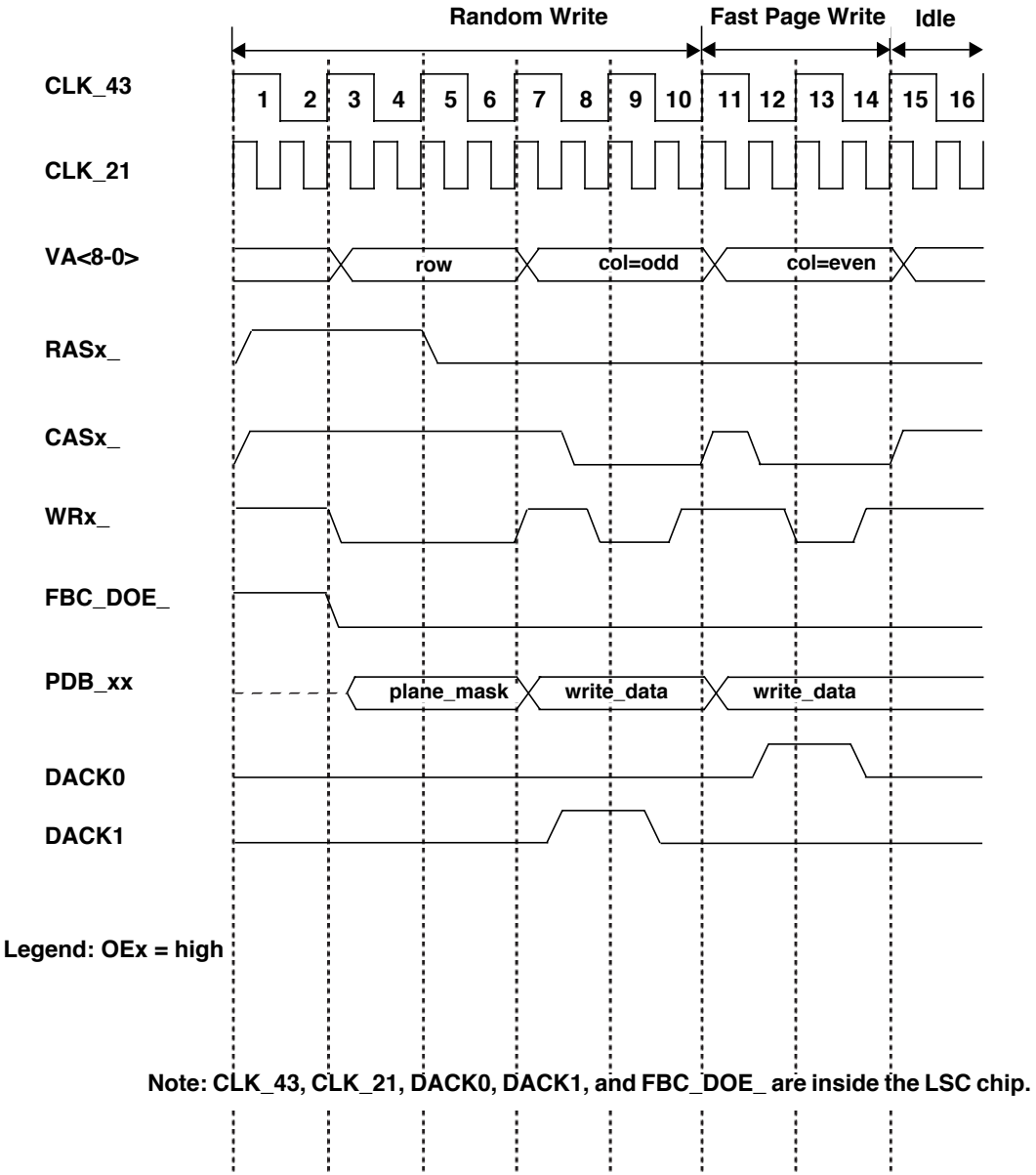


Figure 6-4 DFB to VRAM Random Write, Fast Page Write, Idle (OE_ Controlled Writes)

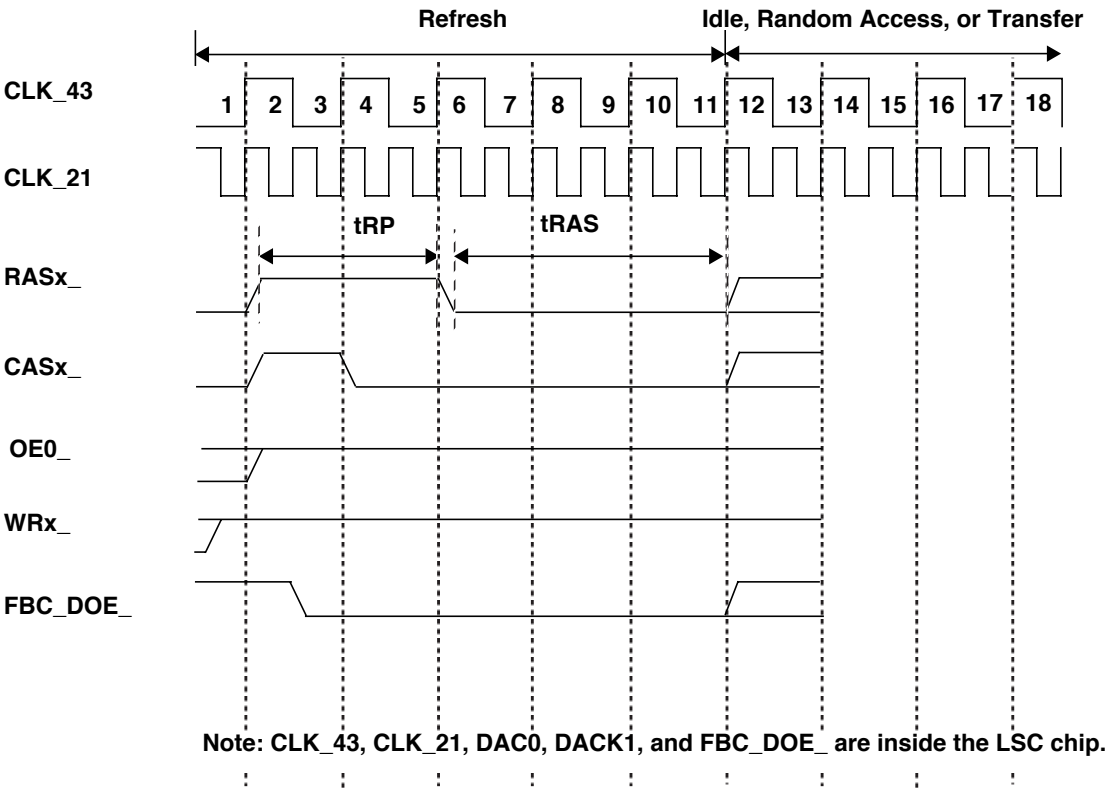


Figure 6-5 CAS_ Before RAS_ Refresh

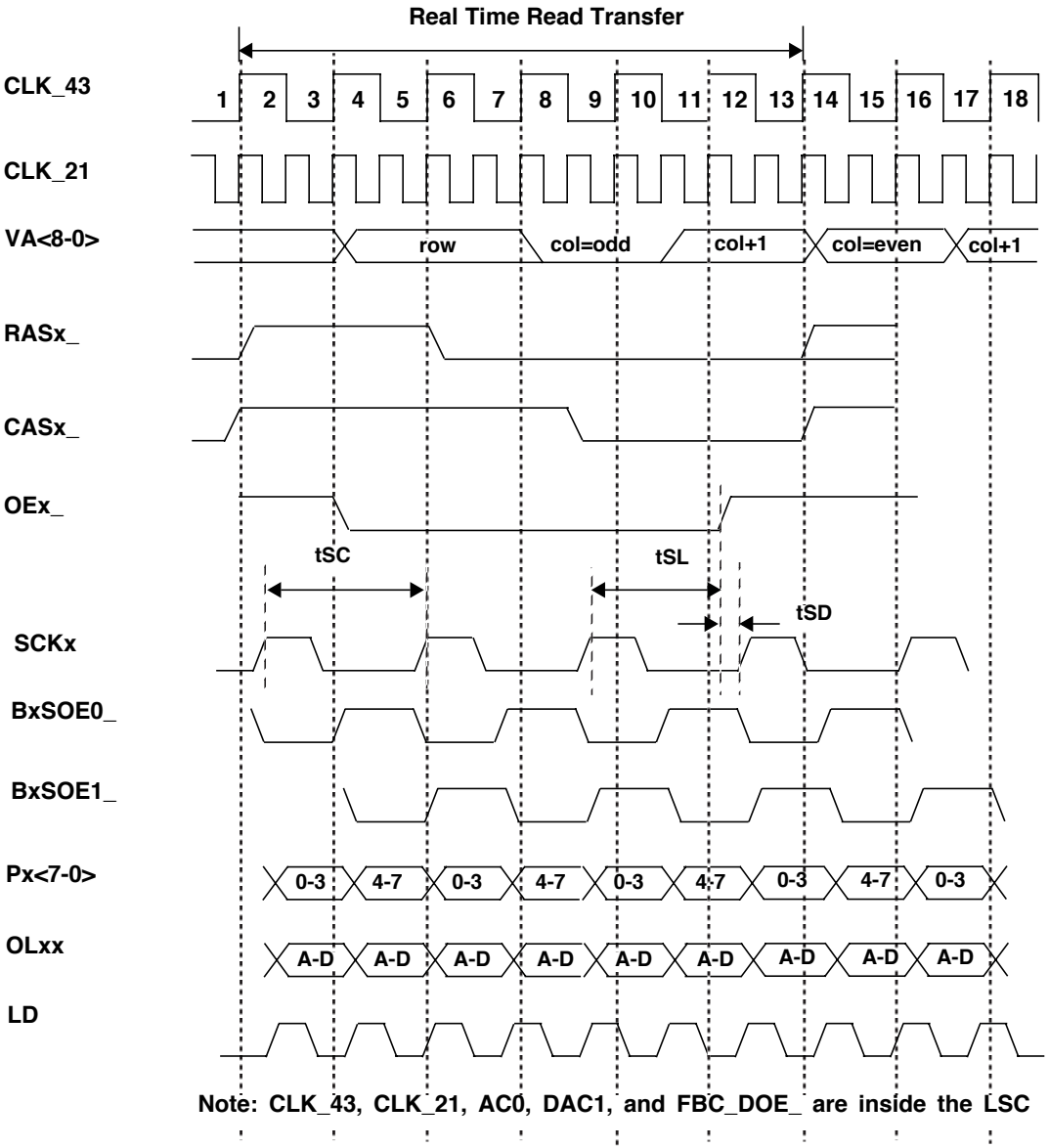


Figure 6-6 Real Time Read Transfer and Serial Read (with 4 Pixel Wide DAC)

Table 6-1 Memory Control AC Characteristics

Symbol	From (Output)	To (Output)	Notes	Min	Max	Unit
Common Timing						
tRP	**RASx_ high**	**RASx_ low**	**High PW**	**80**		**nS**
tCP	CASx_ high	CASx_ low	High PW	20		nS
tRAS	RASx_ low	RASx_ high	Low PW	100		nS
tCAS	CASx_ low	CASx_ high	Low PW	30		nS
tASR	VA[8–0] valid	RASx_ falling	Setup	1		nS
tRAH	RASx_ low	VA[8–0] invalid	Hold	15		nS
tASC	VA[8–0]	CASx_ falling	Setup	1		nS
tCAH	CASx_ low	VA[8–0] invalid	Hold	20		nS
tCSH	RASx_ low	CASx_ high	CAS hold	100		nS
Write Timing						
tWP	WR_ [7–0] low	WR_[7–0] high	Low PW	20		nS
tCWL	WR_ [7–0] low	CASx_ high		30		nS
tRWL	WR_ [7–0] low	RASx_ high		30		nS
tDS	PDBxx[7–0] valid	WR_ [7–0] low	Data Setup	1		nS
tDH	WR_[7–0] low	PDBxx [7–0]	Data hold	25		nS
tMS	PDBxx[7–0] valid	RASx_ low	Setup	1		nS
tMH	RASx_ low	PDBxx[7–0] invalid	Hold	15		nS
Read Timing						
tRAC	RASx_ falling	PDBxx[7-0] valid	RAS Access		100	nS
tCAC	CASx_ falling	PDBxx[7-0] valid	CAS Access		30	nS
tOEA	OEx_ falling	PDBxx[7-0] valid	OE Access		30	nS
tAA	VAx valid	PDBxx[7-0] valid	Address access		50	nS

Table 6-2 Video Related Output Characteristics

Symbol	From (Output)	To (Output)	Notes	Min	Max	Unit
tSC	SCKx high	SCKx high		35		nS
tSL	SCKx high	OEx_ high		10		nS
tSD	OEx_ high	SCKx high		15		nS

6.3 Double Buffered Configurations

Double buffered configurations use WE0_ and WE1_ to externally gate the write lines WRx_ to determine which buffer is written. The LSC can write to buffer0, buffer1 or both. Writes to both buffers are useful for single buffered windows on the same screen as a hardware double buffered window. The single buffered windows are the same in both buffers, so when the buffers are flipped, the single buffered windows do not change on the screen.

The buffer displayed is determined by the pair of VRAM serial output enables that are active. B0SOE0_ and B0SOE1_ control buffer0 while B1SOE_ and B1SOE1_ control buffer1.

Double buffered configurations also have an additional memory access type. When more than one double buffered window is used, flipping the buffers displayed becomes awkward. There is a fast copy mode which allows data to be copied from the hidden buffer to the displayed buffer twice as fast as a normal BLIT. Figure 6-7 shows a fast copy where data is continuously read from buffer0 while it is being written to buffer1. The data goes directly from buffer0 to buffer 1 without passing through the LSC. The write timing is delayed 1/2 clock from read timing to allow the read data to become valid before the write pulse. The staggered CAS* signals indicate that a fast copy is happening. The source and destination addresses must be the same in each buffer during a BLIT to trigger a fast copy.

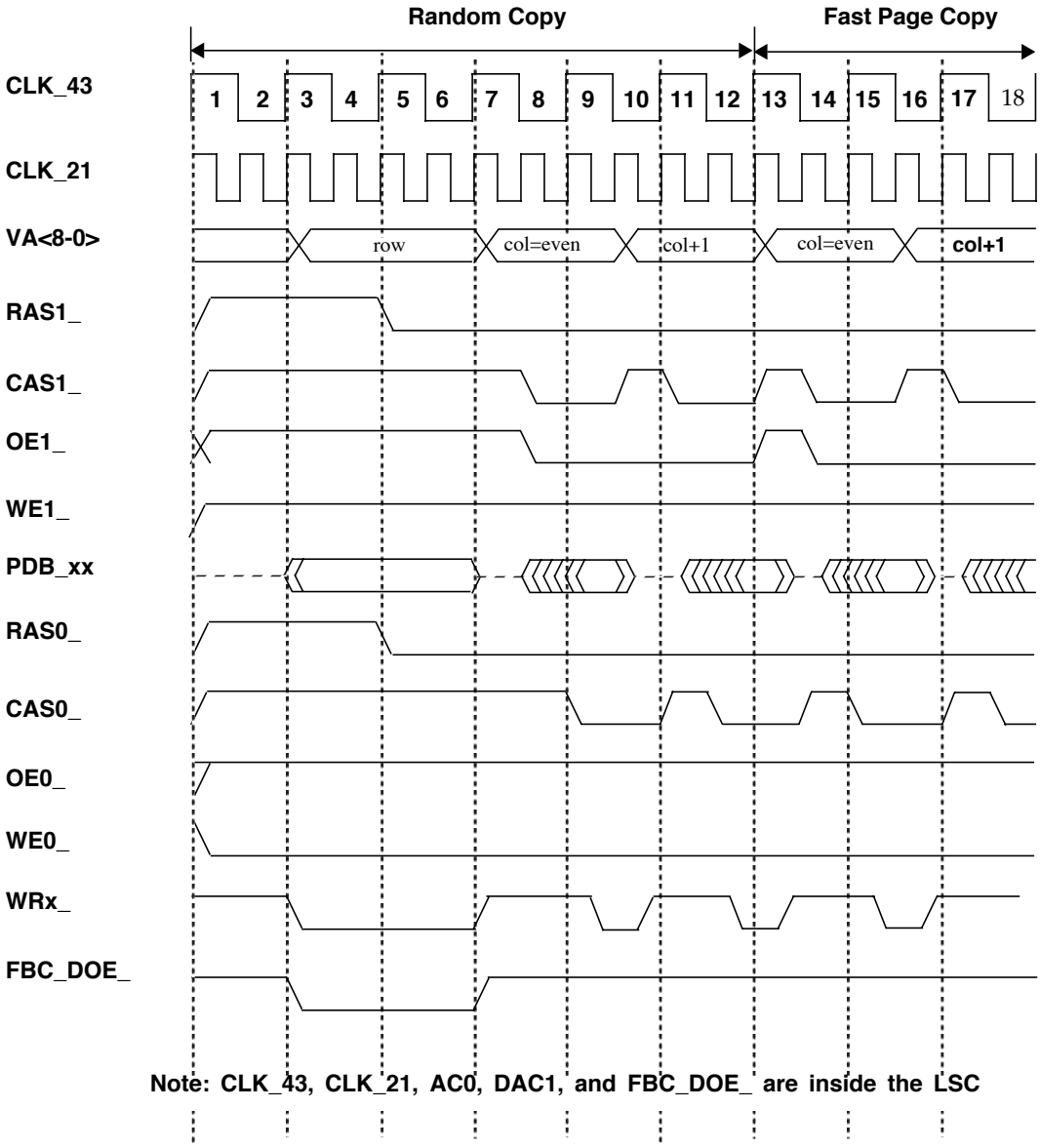


Figure 6-7 Fast Copy From Buffer1 to Buffer0 (for double buffered card)

6.4 Configurations with the 8 Pixel Wide DAC

The LSC supports the high resolution Bt467 DAC which accepts 8 pixels at a time. This DAC is necessary for resolutions beyond 1280 x 1024. Figure 6-8 shows the VRAM serial port timing for configurations with the Bt467 DAC. Eight pixels at a time are shifted out of the VRAM by the shift clock SCKx and loaded into the DAC on the rising edge of LD.

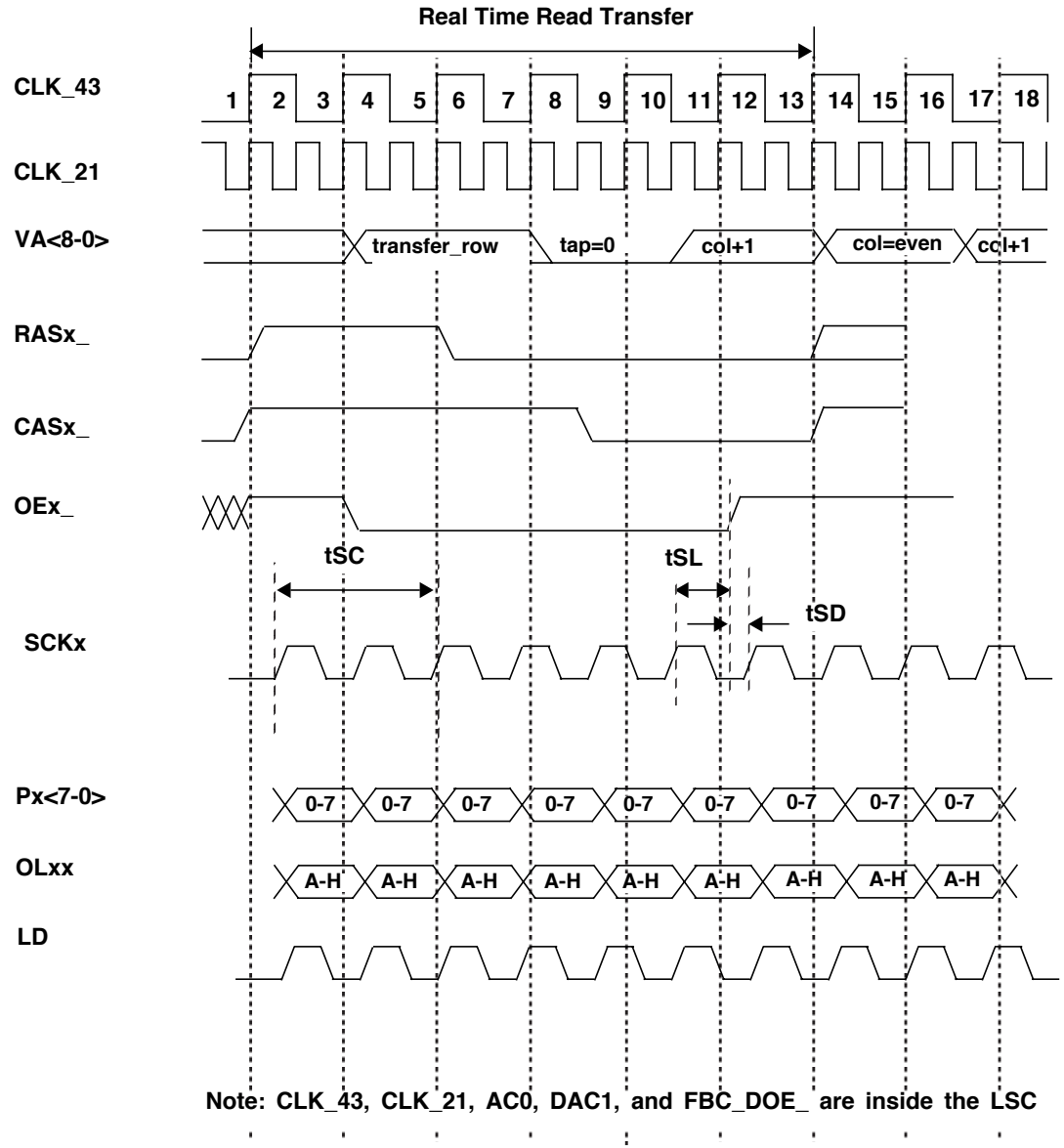


Figure 6-8 Real Time Read Transfer and Serial Read with 8 pixel Wide DAC

6.5 TurboGX Video Memory

The rest of this chapter describes the TurboGX video memory and pertains to the TurboGX card only. It provides the functional description of the video memory architecture, data side timing, and video side timing.

6.6 TGX Memory Architecture

The TGX chip supports four different memory configurations:

- 1 megabyte with eight 128k x 8 60 nS VRAMs
- 2 megabytes high resolution single buffer with 8 256k x 8 60 nS, or 16 256k x 4 60 nS VRAMs
- 2 megabytes low resolution double buffer or high resolution single buffer with 16 128k x 8 60 nS VRAMs
- 4 megabytes high resolution double buffer with 16 256k x 8 60 nS, or 32 256k x 4 60 nS VRAMs

Refer to Chapter 8 “Single Chip GX Cards Configurations” for block diagrams of memory architecture for a particular board.

6.6.1 Data Side Architecture

The video address (VA<8..0>) is common to all memory chips regardless of configuration. TurboGX configuration consists of 16 256k x 8 memory chips. The address is multiplexed in the form of a VRAM row address and column address. The VRAM rows do not correspond to scan lines on the screen. There is a new row address every 4096 pixels. The VRAMs have an extended fast page mode which allows faster accesses if the row address does not change. The VRAMs remember the row address, so subsequent addresses anywhere within the current row only require a column address and a column address strobe (CAS0* for bank 0 and CAS1* for bank 1). A fast page mode read from the frame buffer takes three cycles (60ns) in the single buffer mode, and two cycles (40 nS) in the double buffer mode, where accesses to the buffers are interleaved. A non-page mode read takes seven cycles (140 nS). A fast page mode write takes two cycles (40ns) in the single buffer mode and one cycle (20ns) in the double buffer mode. A non-page mode write takes six cycles (120 nS). In all cases, changing the row address adds a three cycle (60 nS) penalty to the access time.

6.6.2 Video Side Architecture

Note that the serial input to the Palette DAC is 64 bits wide. Therefore, the serial output data from the Video Memory to the Palette DAC must be interleaved 2 to 1. During the SOE0* output enable signal, bits 0 through 7 of pixels 0 through 7 are transferred to the Palette DAC on signal lines PA<7.. 0> through PH<7.. 0>, respectively. Then the SOE1* signal enables pixels 8 through 15 on the same signal lines.

6.7 Data Side Timing

and Table 6-2 show the most important timing requirements for VRAM used with the TGX chip. The memory control parameters are illustrated in Figure 6-9 through Figure 6-22, and the video related parameters are illustrated in Figure 6-23 through Figure 6-28.

6.7.1 Read Cycle

The TGX has one common random read cycle and two types of fast page read cycles, for either the single buffer mode or double buffer mode.

The random read starts with a RAS* precharge high pulse lasting 2.5 clocks (50 nS). On the falling edge of RAS*, OEx must be high and WE_DSFx must be low. At that time, the row address from the 9-bit VRAM address bus VA<8..0> is latched into the memory chip. If WBx_, write-per-bit, is low at the falling edge of the RAS*, then the pixel plane mask inside the VRAM is updated with the new mask on the PDBx_x<7..0> bus. The plane mask is only used for writing to the VRAM, but it is simpler to update it for every random access. See Figure 6-9 and Figure 6-10.

The falling edge of CASx* latches in the column address. CASx* low and OEx* low enable the VRAM data outputs onto the PDBx_x bus. The read data will be valid after tRAC, tAA, tCAC, and tOEA are satisfied. Typically, the data will be valid 15 nS after the falling edge of OEx* at the VRAM assuming tOEA = 15 nS.

The random read cycle described above applies for both the single buffer mode and double buffer mode. In a fast page read cycle, the VRAMs only require the new column address which is latched at the falling edge of CASx*. In the single buffer mode, TGX can do this at every three clock cycles: two clocks for the CASx* pulse and one clock idled to wait for data out. In the double buffer

mode, the idling clock can be eliminated by interleaving the two banks. Now a fast page read from the frame buffer will only take two clock cycles. See Figure 6-11 and Figure 6-12.

6.7.2 Write Cycle

The TGX has one common random write cycle and two types of fast page write cycles, for either the single buffer mode or double buffer mode. These cycles accommodate both the “FBC” and “DFB” write cycles from the original GX card which had separate chips, such as the Frame Buffer Controller and Dumb Frame Buffer modules, for different functions.

The random write cycle starts with a RAS* precharge high pulse just like the random read. With WBx_ low, the falling edge of RAS* latches in the row address and a new plane mask. The plane mask determines which bits of the pixel will be written, hence write-per-bit. FBC writes use the write-per-bit mode, while DFB writes use the normal write mode. For a DFB write, WBx_ stays high at the falling edge of RAS*, writing without any mask. See Figure 6-13 and Figure 6-14.

While WE_DSFx is low, the falling edge of CASx* latches in the column address. The TGX can use either early writes or OE controlled writes. Late write means that the write data is not latched into the VRAM until the falling edge of the write enable WRx_. The write lines WR<7..0>_ determine which of the 8 pixels are actually written to the VRAM. Any combination of pixels can be enabled using a pixel mask register inside the TGX.

FBC writes are no longer double accessed. The random write cycle described above applies for both the single buffer mode and double buffer mode. In a fast page write cycle, the VRAMs only require the new column address which is latched at the falling edge of CASx*. In the single buffer mode, TGX can do this at every two clock cycles: one clock for the CASx* pulse and one clock idled for CASx precharge. In the double buffer mode, the idling clock can be eliminated by interleaving the two banks. Now a fast page write from the frame buffer will only take one clock cycle. See Figure 6-15 and Figure 6-16.

A dead state is required to change the direction of the pixel data bus from a read to a write. A dead state is not required when going from write to read because all read cycles have a half clock of dead time built into the beginning of the cycle. See Figure 6-17 and Figure 6-18.

6.7.2.1 Load Color Register and Block Write Cycle

For faster window clearing, the TGX uses block writes in addition to the normal writes. In the block write mode, the TGX can write into four consecutive column locations in the same page, with data previously loaded in the color register.

The load color register cycle is initiated with OEx_, WRx_, and WE_DSFx all held high at the falling edge of RAS*. Then at the falling edge of CASx*, WRx_ drops low and the color data is loaded from the PDBx_x bus into the internal color register. The entire cycle requires six clock cycles, regardless of single or double buffer mode. See Figure 6-19 and Figure 6-20. The data stored will be used by block writes till the next load color register cycle.

At the falling edge of RAS*, the row address is latched in the memory chip, and the memory cells in that page will be refreshed during the load color register cycle. Thus, the first access after a load color register cycle is forced to be a non-page mode access.

A block write is initiated like a random write-per-bit cycle. The plane mask is latched at the falling edge of RAS*, and the column select is provided at the falling edge of CASx* or WRx_, whichever one is later. At the falling edge of CASx*, WE_DSFx must be low; this also applies in the fast page block write mode. See Figure 6-13 through Figure 6-16. The length of a random and fast page block write cycle is similar to that of a normal random and fast page write cycle.

During block write, only the seven most significant bits of the column address are latched in at the falling edge of CASx*. The last two bits of the column address can be encoded from the four bit column mask data taken from the PDBx_x bus. These four bits mask which four consecutive column locations are to be written; all four locations must be in the same page.

6.7.3 Refresh

Video RAM is a dynamic memory with tiny capacitors as storage cells which must be recharged periodically. The 2 Meg VRAMs supported by TGX need to be refreshed entirely every 8 mS. TGX does this by refreshing one of the 512 rows every 15.6 mS. The refresh cycle is a CAS before RAS CBR style which takes six clocks (120 nS). See Figure 6-21 and Figure 6-22. CBR auto refresh uses

a row counter inside each VRAM to determine the row to be refreshed. Refresh overwrites the row address stored in the VRAM, so the first access after a refresh is forced to be a non-page mode access.

6.7.4 Video Transfer

Video RAMs are dual ported with a serial port as well as a random access port. There is a serial access memory that is loaded in parallel with one row of data, then shifted out while the TGX is using the random port. The parallel loading is done by either a self-timed read transfer cycle or a split read transfer cycle.

The TGX uses the self-timed read transfer cycle during vertical blanking to reset and determine the absolute TAP address location. Tap is the start address of the serial pointer of the shifter. The self-timed read transfer is issued only at vertical blanking because of the synchronization restriction between the random port control signals and the shift clock. At all other times, a split read transfer is preferred because it eliminates this requirement.

The falling edge of OE* while RAS* is high, signals the start of the transfer cycle. At the falling edge of RAS*, WE_DSFx must be low to qualify for a self-timed read transfer cycle, and at the same time the transfer row address is latched into the VRAM by the falling edge of RAS*. When CASx* drops, it latches in the TAP address which is always 0 in a read transfer cycle. The trailing edge of OE* triggers the actual data transfer from the main memory to the serial access memory. The entire cycle takes six clock cycles. See Figure 6-23 and Figure 6-24. The self-timed transfer cycle is issued during vertical blanking, where the shift clock is continuously held low, so the dual port timing synchronization restriction is minimized.

A split transfer cycle is initiated the same way, but at the falling edge of RAS*, WE_DSFx must be high. Also when CASx* drops, it latches in the TAP address, which in a split transfer cycle, toggles between 0 and 256. There is no dual port timing synchronization restriction, the split read transfers are only restricted from being issued too closely to the divided boundaries of the shifter. The TGX divides the shifter in halves, such that a split read transfer can occur inside a 256 shift clock window (a minimum of 1.18 mS, with 216 MHz shift clock for HiRes). The split read transfer cycle only takes six main clock cycles (120 nS). See Figure 6-23 and Figure 6-24. The split read transfer occurs every 2048 pixels in 256k x8 VRAM configurations.

6.8 Serial Timing to DAC

The TGX supports the high resolution Bt467 DAC which accepts 8 pixels at a time. This DAC is necessary for resolutions beyond 1280 x 1024. Figure 6-25 through Figure 6-28 show the serial port read timing. The shift clock SCKx advances the serial shifter in all the VRAMs at once. Since the TurboGX is a double buffered frame buffer, it alternates the serial output enables BxSOE0_ and BxSOE1_ to enable a set of eight pixels from each buffer onto the pixel bus Px<7..0>.

6.9 Double Buffering

With the 16 256k x 8 VRAMs configuration, the TGX can read and write to either buffer0, buffer1 or both. To access both buffers, it interleaves the memory access cycles to eliminate any idling clocks. This is useful for single buffered windows such that when the buffers are flipped, the single buffered windows do not change on the screen.

When more than one double buffered window is used, flipping the buffers displayed becomes awkward. Fast page read and write allows data to be copied from the hidden buffer to the displayed buffer.

The buffer displayed is determined by the pair of VRAM serial output enables that are active. B0SOE0_ and B0SOE1_ control buffer0 while B1SOE_ and B1SOE1_ control buffer1.

Table 6-3 Memory Control AC Characteristics

Symbol	From (Output)	To (Output)	Notes	Min	Max	Unit
Common Timing						
tRP	RASx_ high	RASx_ low	High PW	50		nS
tCP	CASx_ high	CASx_ low	High PW	20		nS
tRAS	RASx_ low	RASx_ high	Low PW	70		nS
tCAS	CASx_ low	CASx_ high	Low PW	20		nS
tCSH	RASx_ low	CASx_ high	CAS hold	60		nS
tASR	VA[8–0] valid	RASx_ falling	Setup	0		nS
tRAH	RASx_ low	VA[8–0] invalid	Hold	10		nS
tASC	VA[8–0]	CASx_ falling	Setup	0		nS
tCAH	CASx_ low	VA[8–0] invalid	Hold	10		nS

Table 6-3 Memory Control AC Characteristics

Symbol	From (Output)	To (Output)	Notes	Min	Max	Unit
tFSR	WE_DSFx valid	RASx_ low	Setup	0		nS
tRFH	RASx_ low	WE_DSFx invalid	Hold	10		nS
tFSC	WE_DSFx valid	CASx_ low	Setup	0		nS
tCFH	CASx_ low	WE_DSFx invalid	Hold	10		nS
Write Timing						
tWP	WR_ [7–0] low	WR_[7–0] high	Low PW	14		nS
tCWL	WR_ [7–0] low	CASx_ high		20		nS
tRWL	WR_ [7–0] low	RASx_ high		30		nS
tDS	PDBxx[7–0] valid	WR_ [7–0] low	Data Setup	0		nS
tDH	WR_[7–0] low	PDBxx [7–0]	Data hold	10		nS
tMS	PDBxx[7–0] valid	RASx_ low	Setup	0		nS
tMH	RASx_ low	PDBxx[7–0] invalid	Hold	10		nS
Read Timing						
tRAC	RASx_ falling	PDBxx[7-0] valid	RAS Access		70	nS
tCAC	CASx_ falling	PDBxx[7-0] valid	CAS Access		30	nS
tOEA	OEx_ falling	PDBxx[7-0] valid	OE Access		30	nS
tAA	VAx valid	PDBxx[7-0] valid	Address access		30	nS

Table 6-4 Video Related Output Characteristics

Symbol	From (Output)	To (Output)	Notes	Min	Max	Unit
tSCC	SCKx high	SCKx high		37		nS
tTSD	DT high	SCKx high		>>10		nS
tSTS	SCKx high	RASx low		>>25		nS

6.10 Timing diagrams

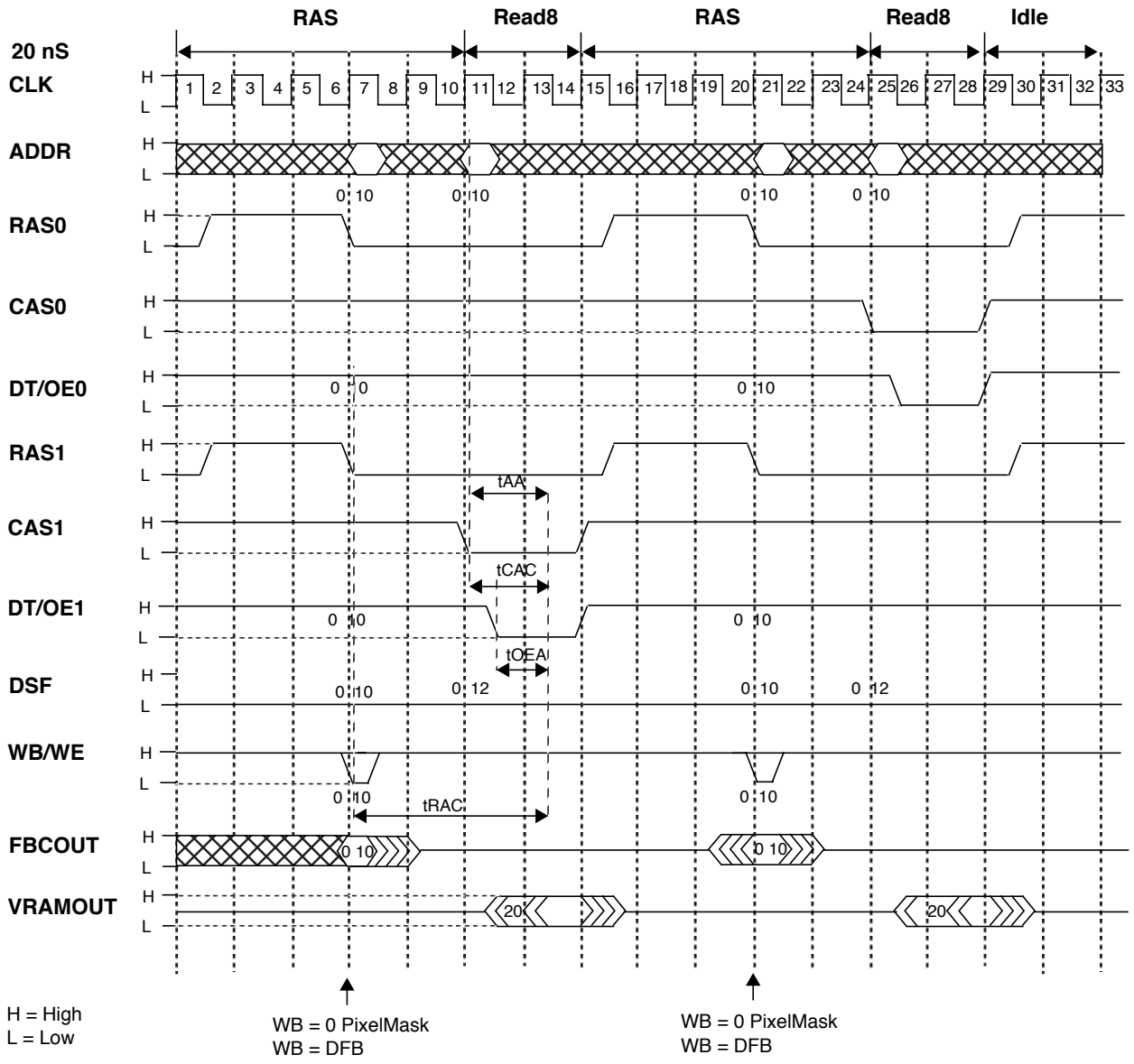


Figure 6-9 VRAM Two Bank Random Read Cycle (140 nS)

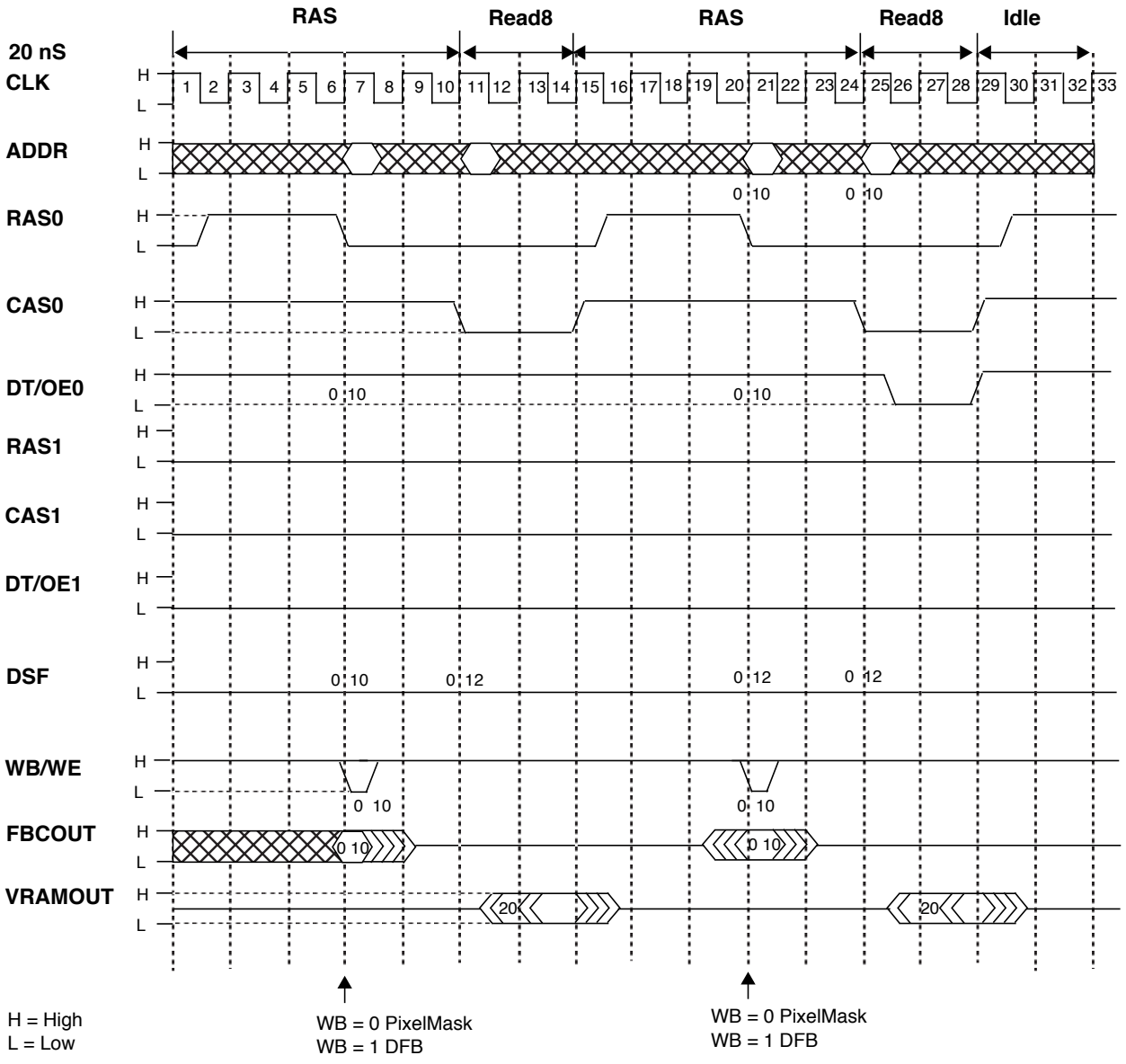


Figure 6-10 VRAM One Bank Random Read Cycle (140 nS)

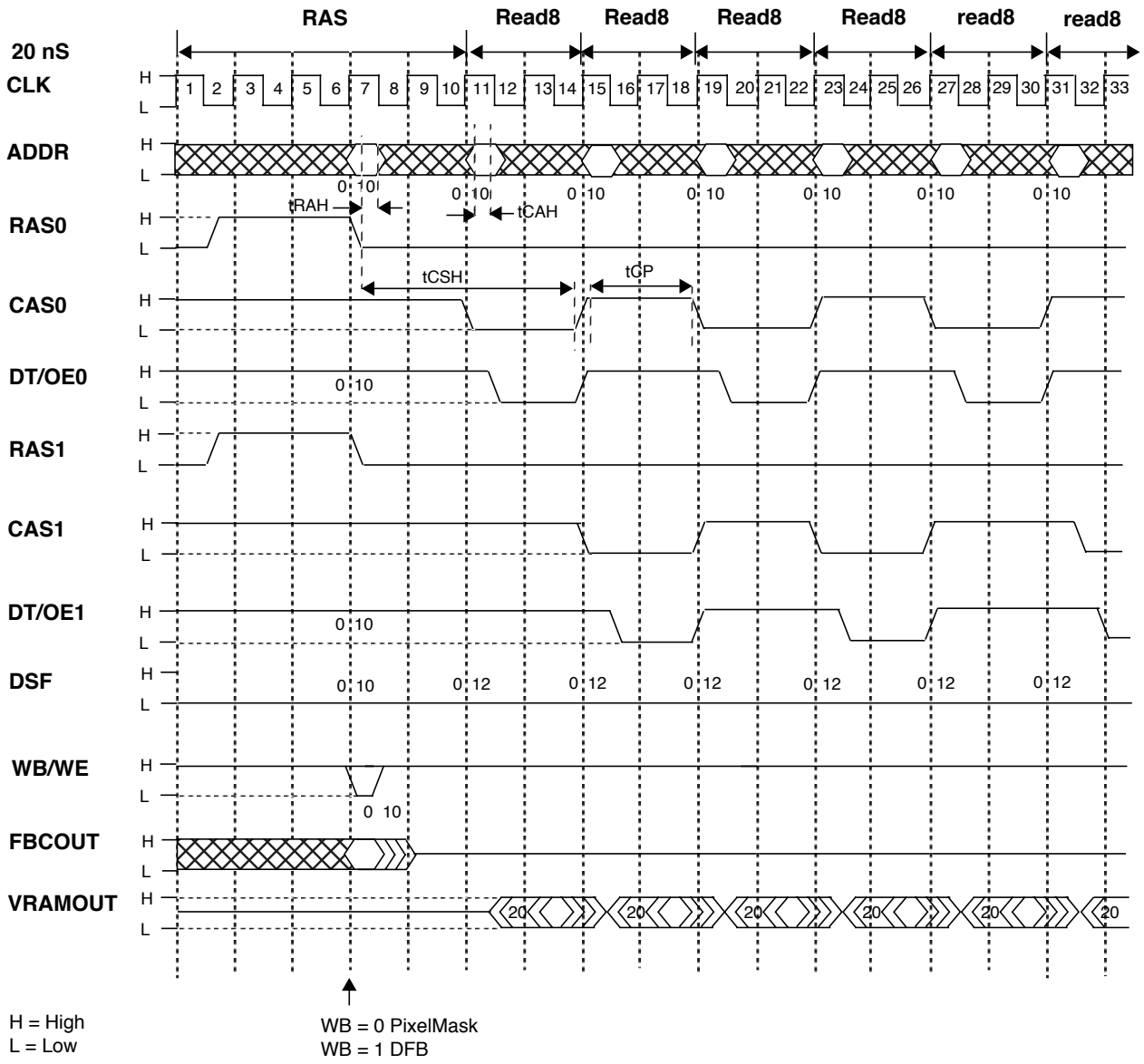


Figure 6-11 VRAM Two Bank Fast Page Mode Read Cycle (40 nS)

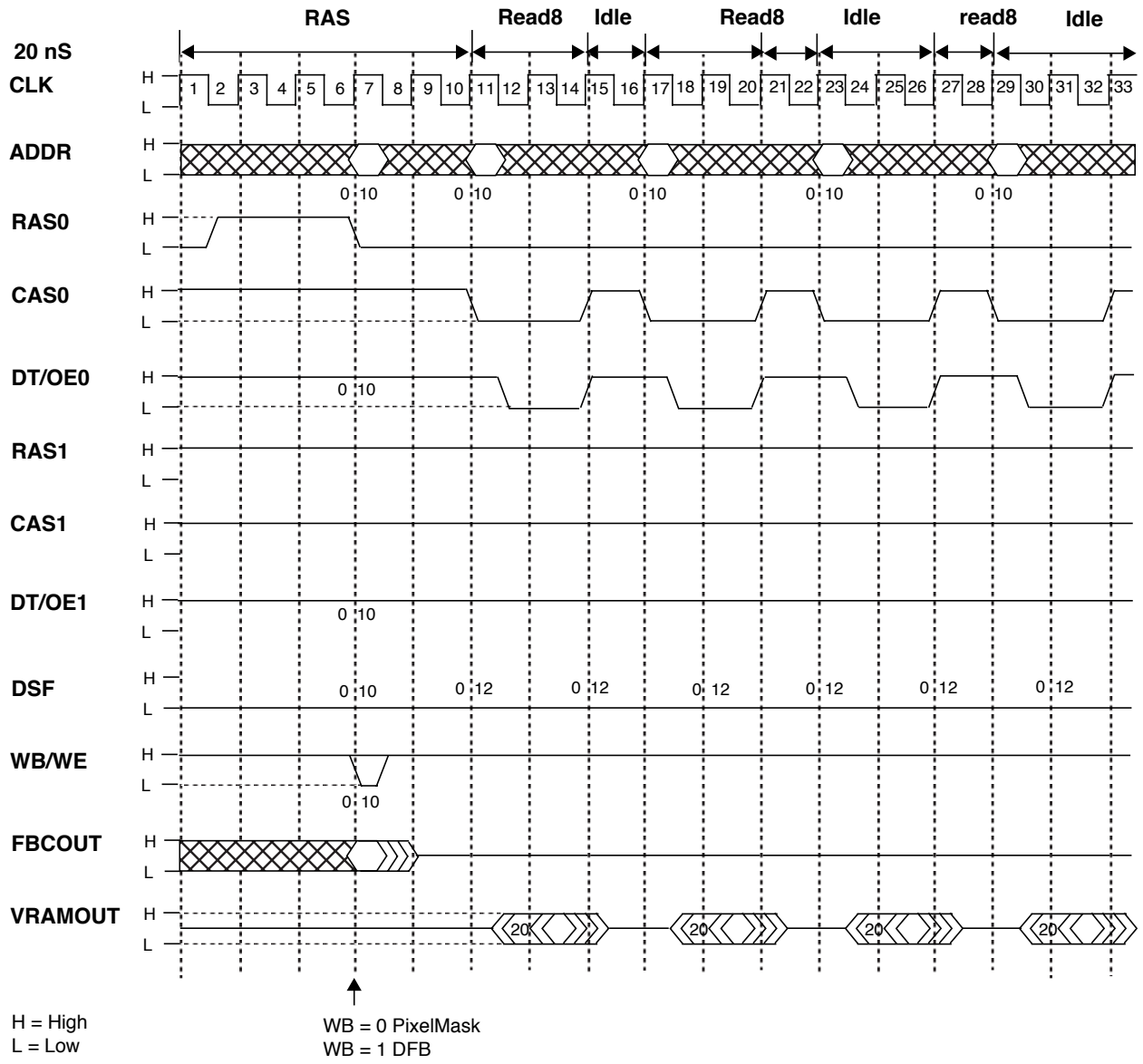


Figure 6-12 VRAM One Bank Fast Page Mode Read Cycle (60 nS)

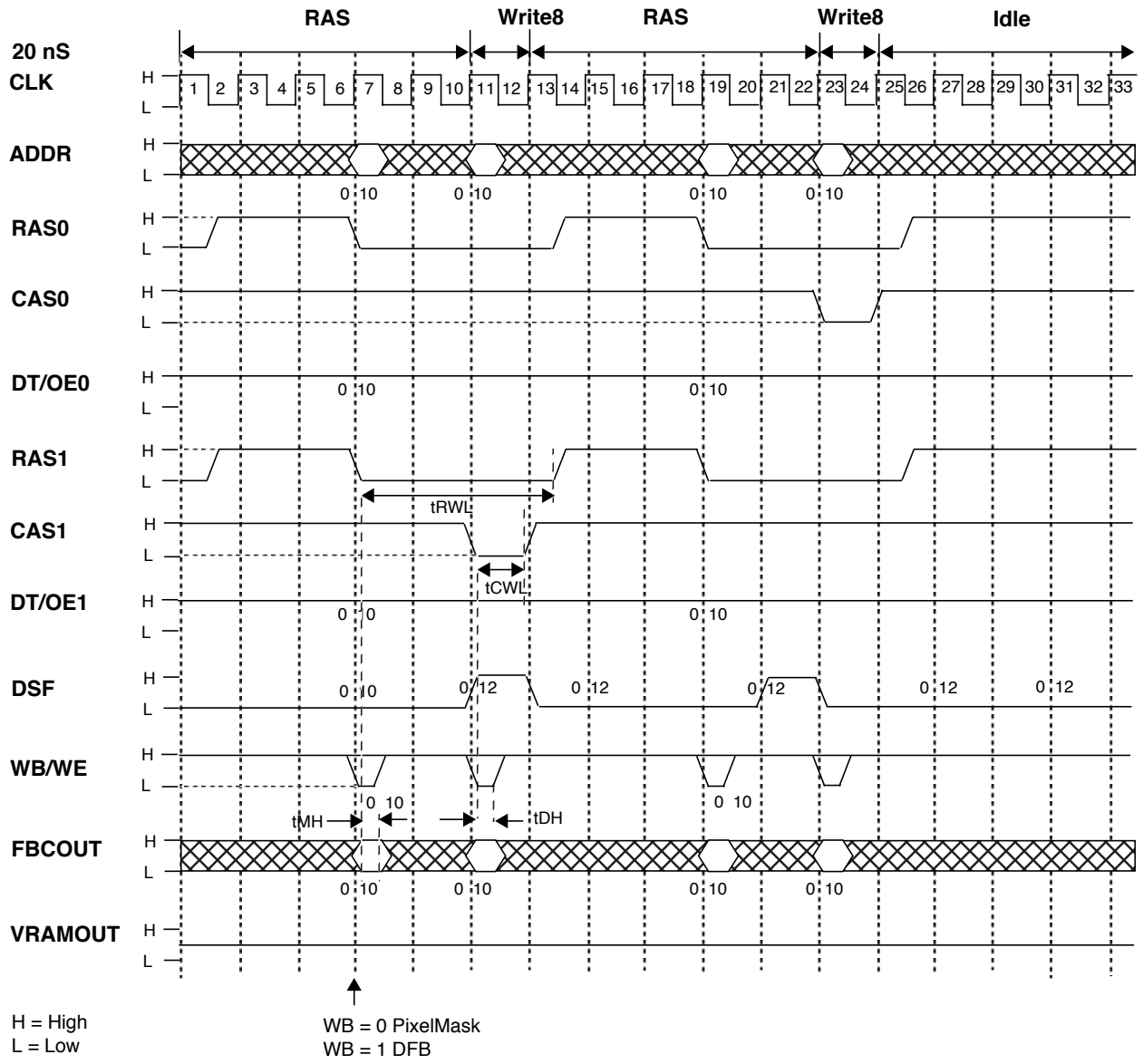


Figure 6-13 VRAM Two Bank RandomWrite Cycle (120 nS)

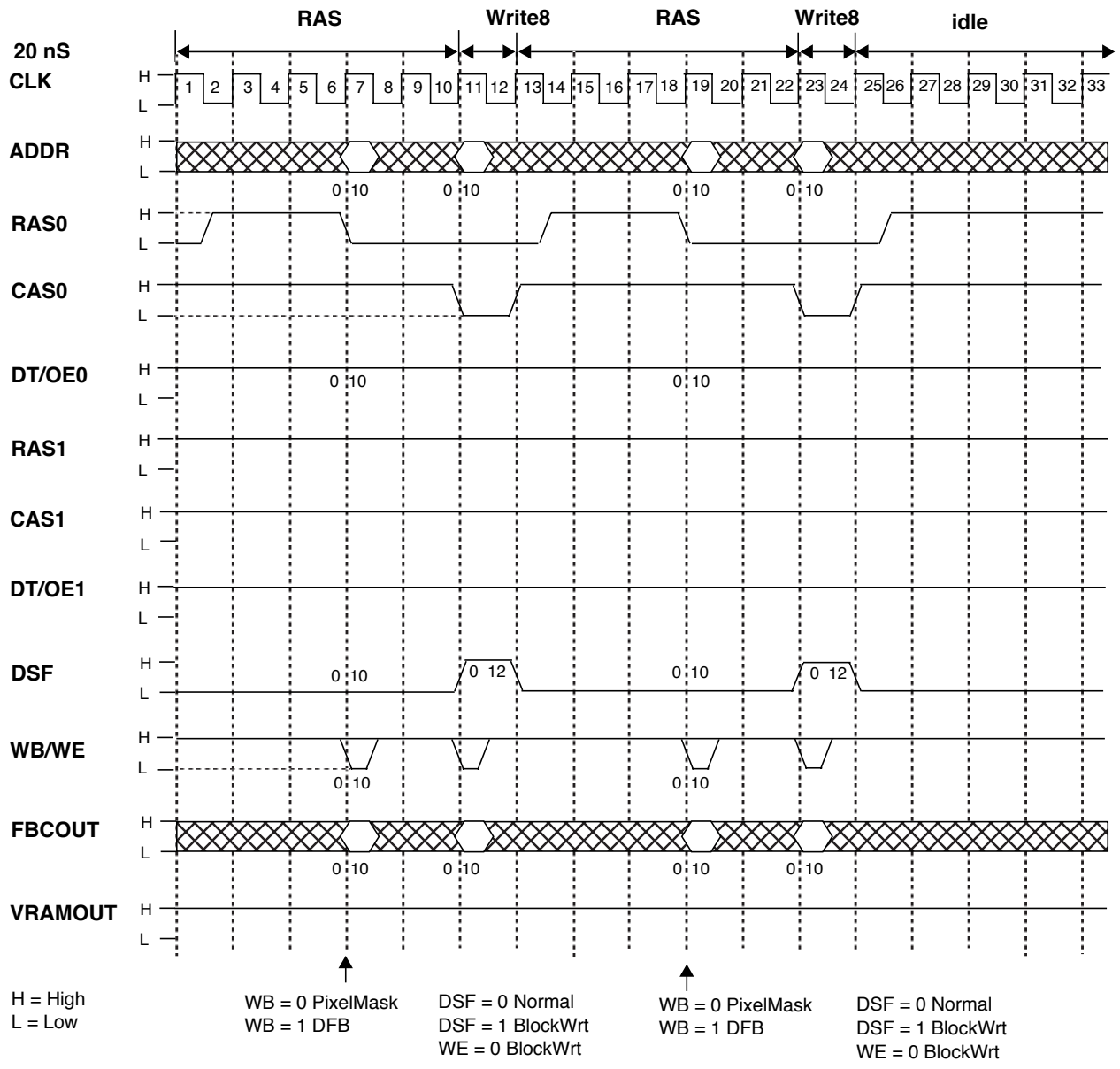


Figure 6-14 VRAM One Bank RandomWrite Cycle (120 nS)

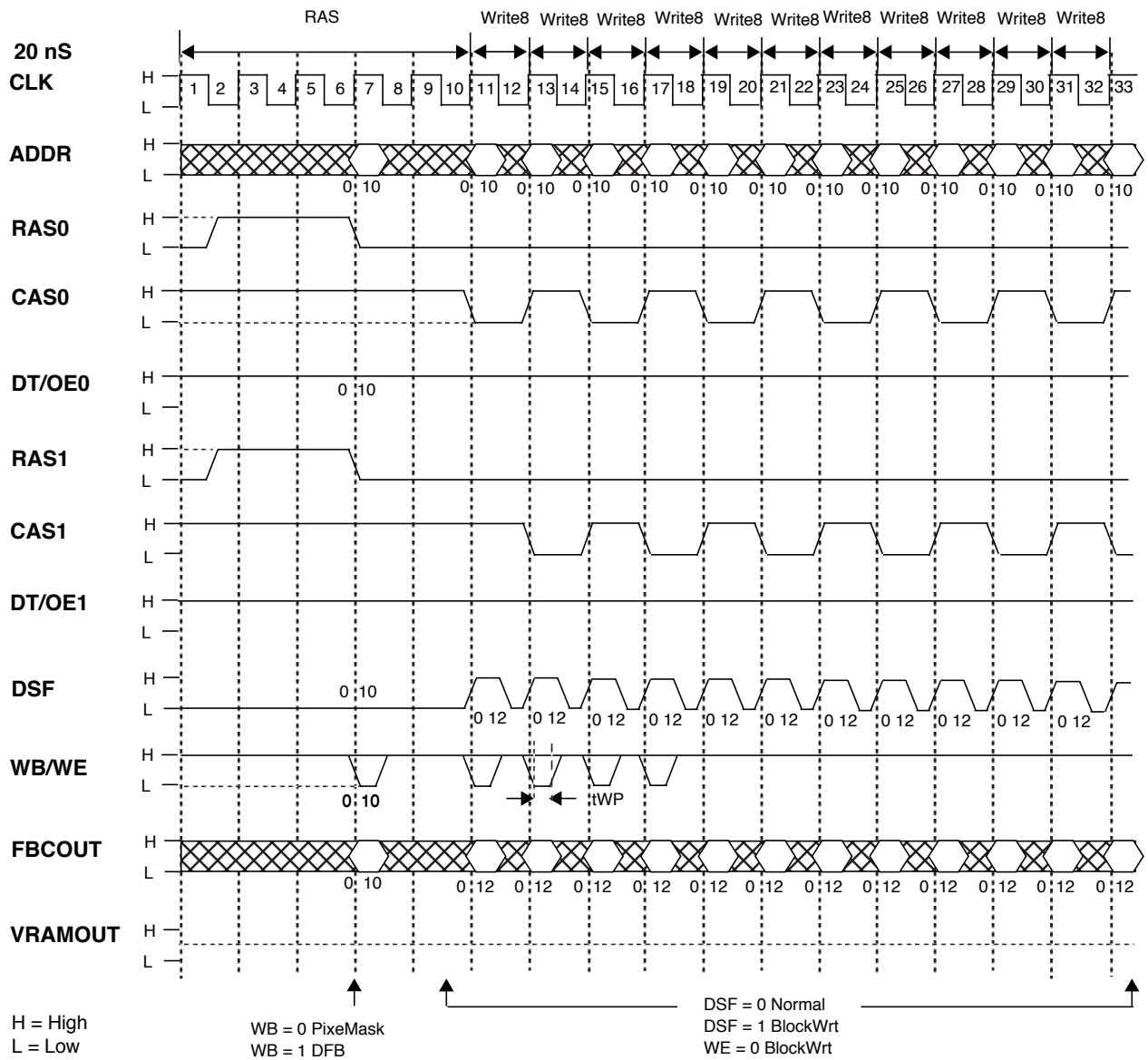


Figure 6-15 VRAM Two Bank Fast Page Write Cycle (20 nS)

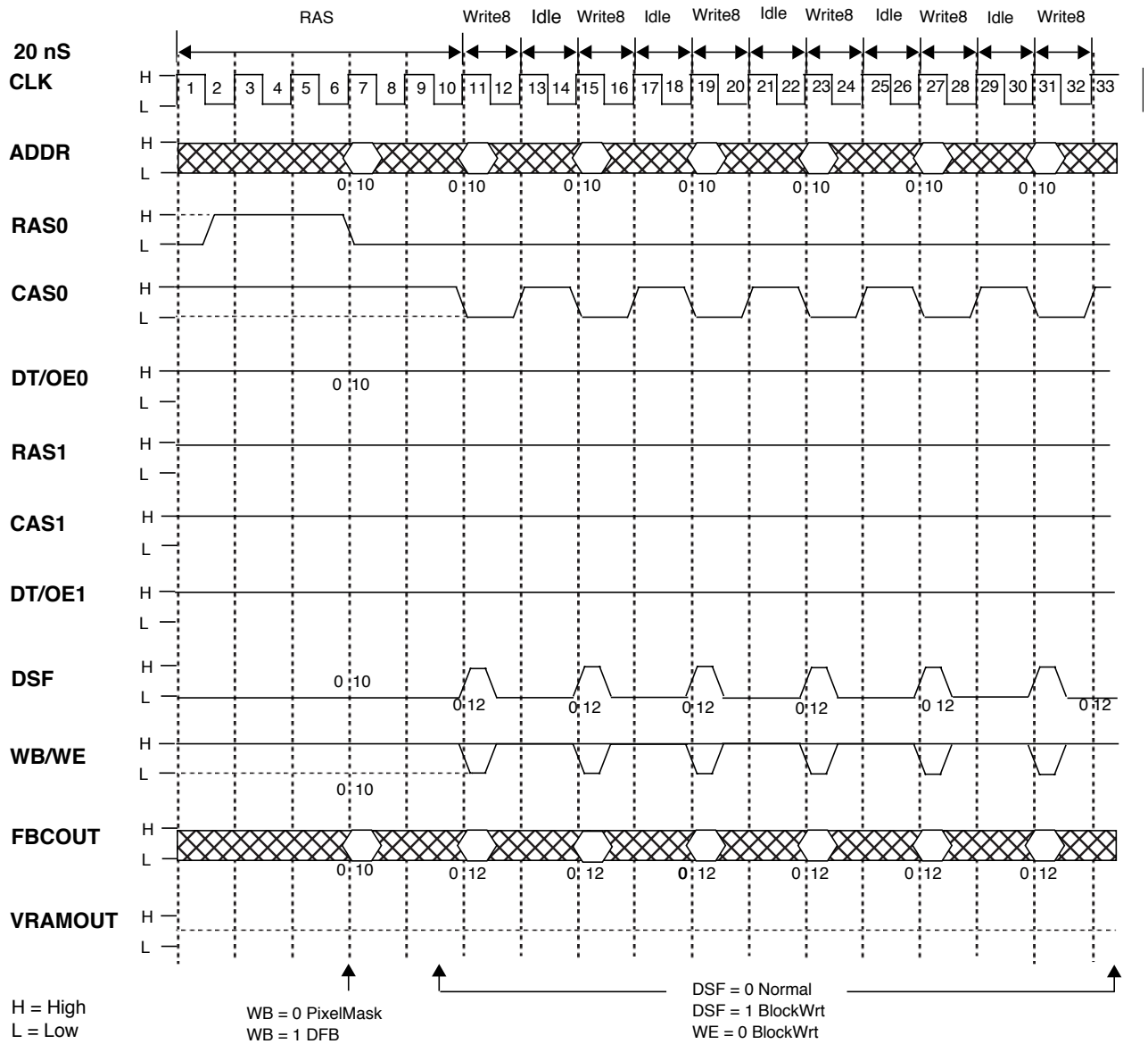


Figure 6-16 VRAM One Bank Fast Page Write Cycle (40 nS)

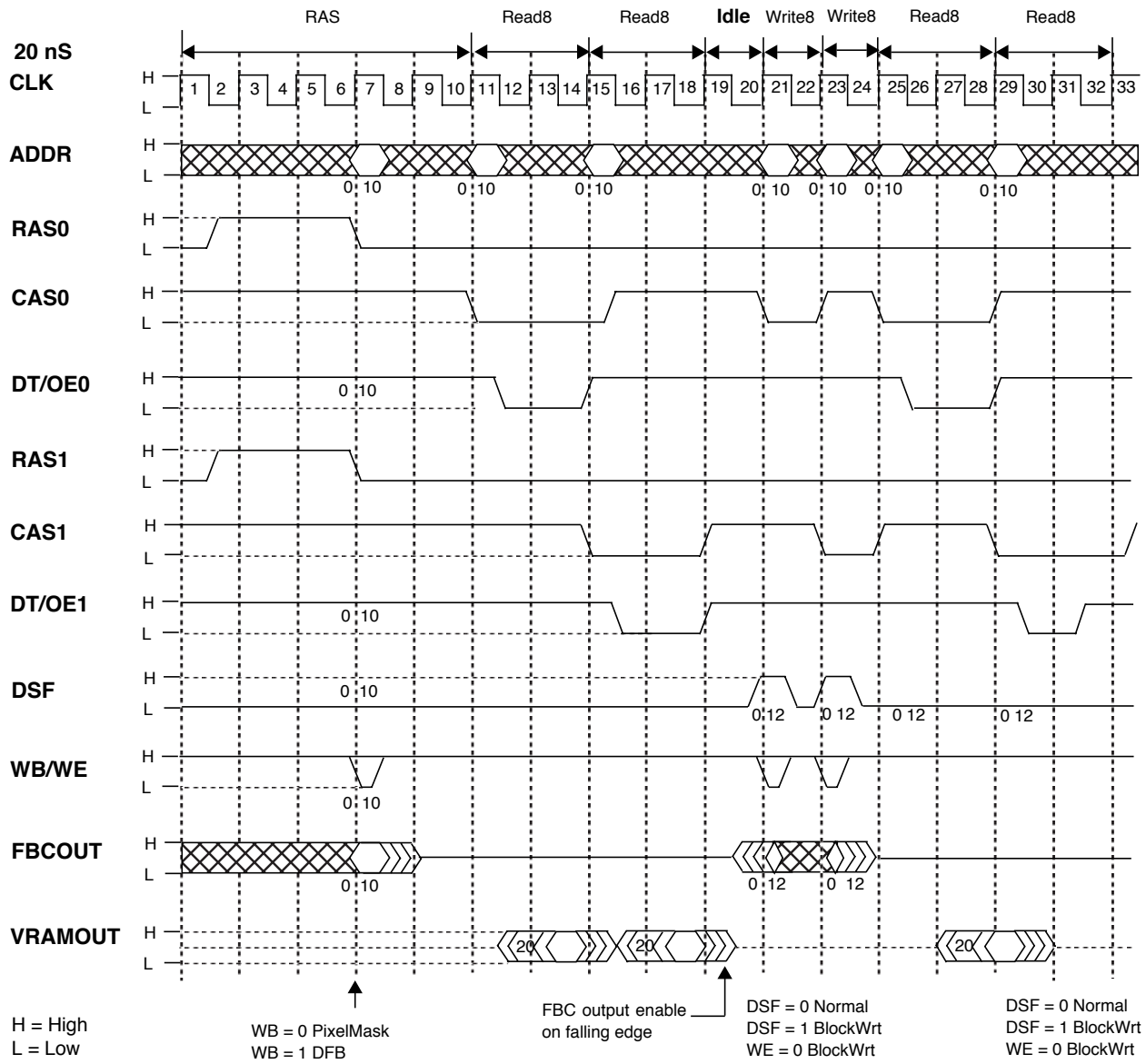


Figure 6-17 VRAM Two Bank Read and Two Bank Write Cycle (200 nS, 140 nS)

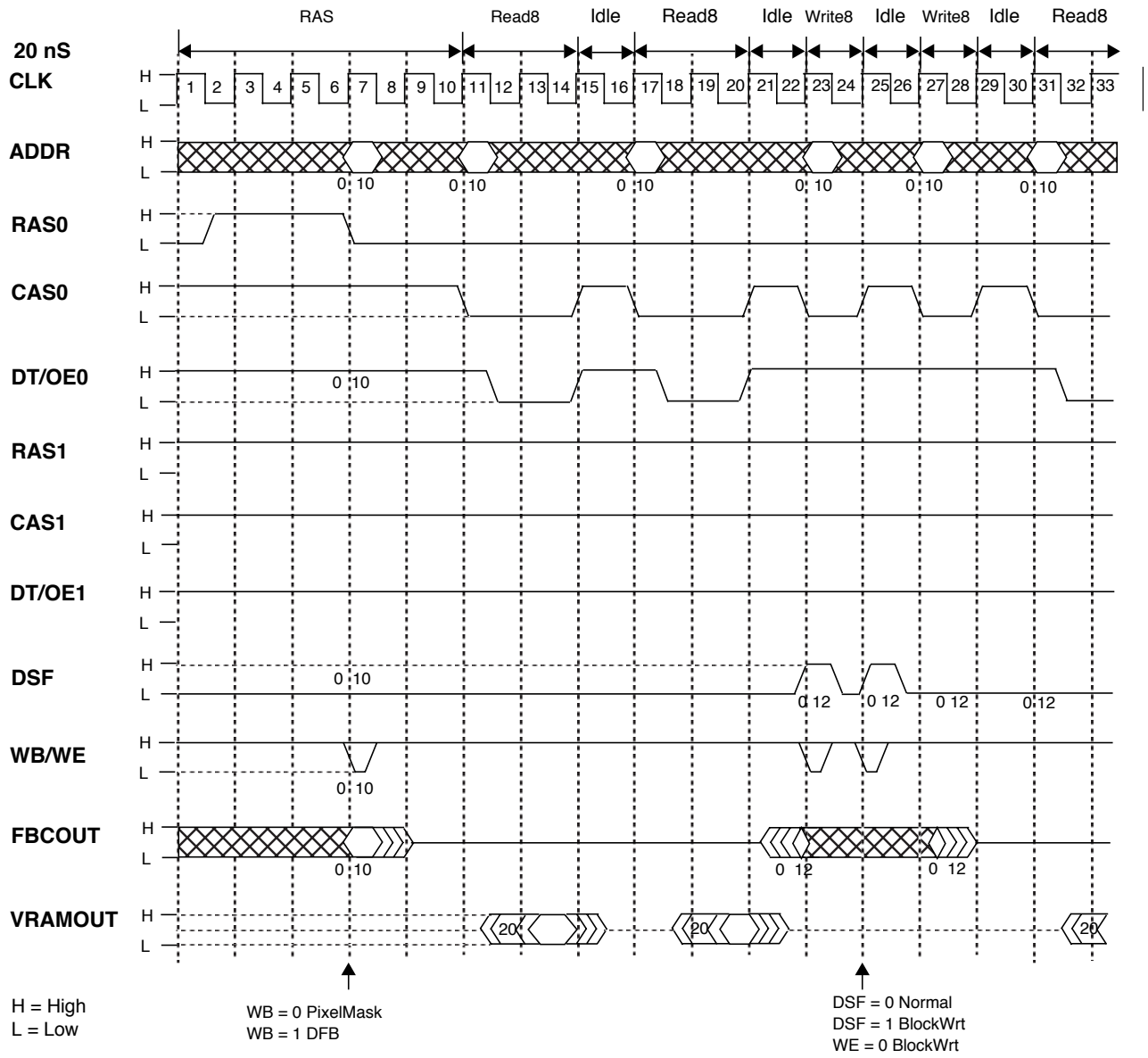


Figure 6-18 VRAM One Bank Read and One Bank Write Cycle (260 nS, 200 nS)

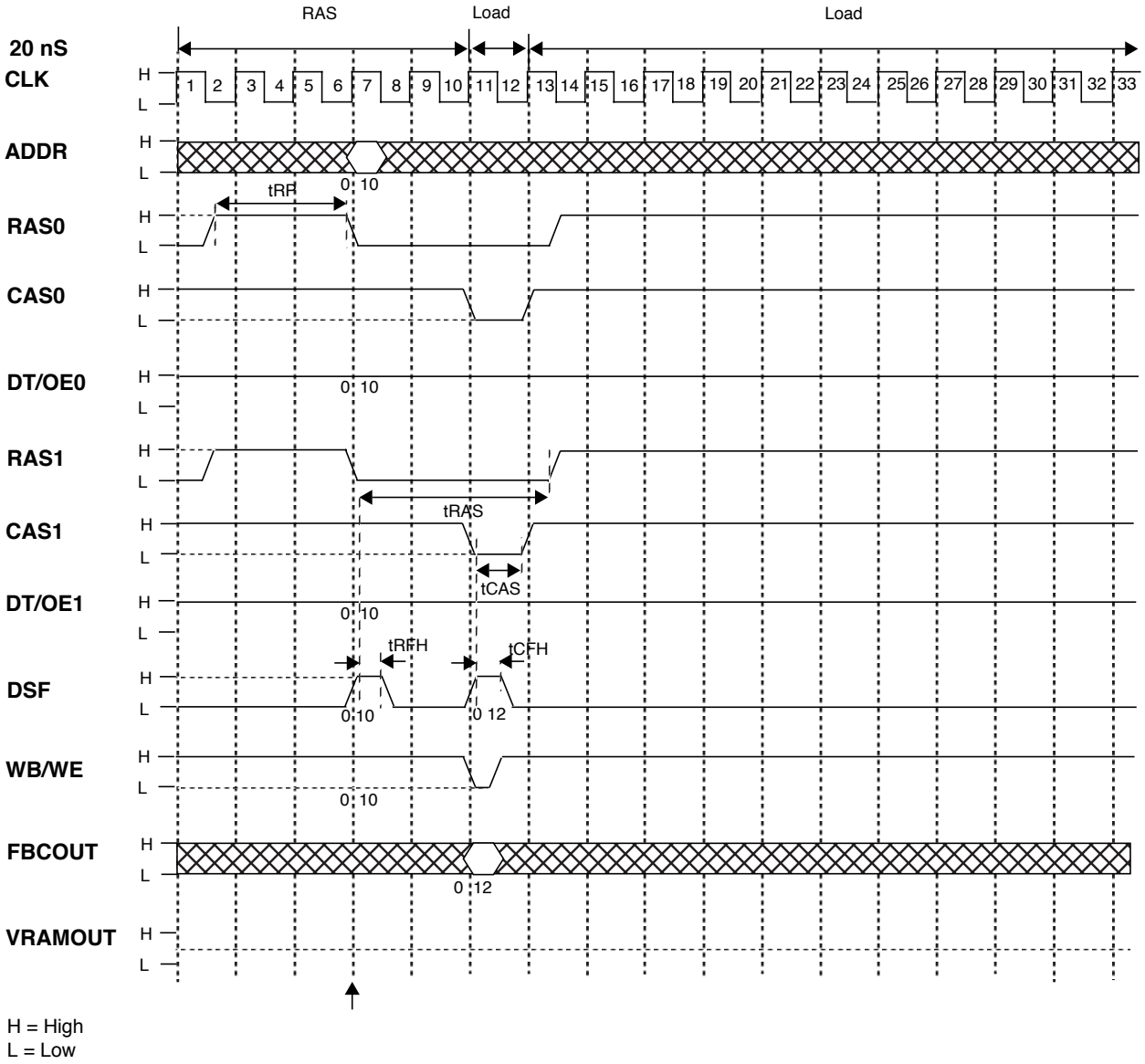


Figure 6-19 Two Bank Load Color (120 nS)

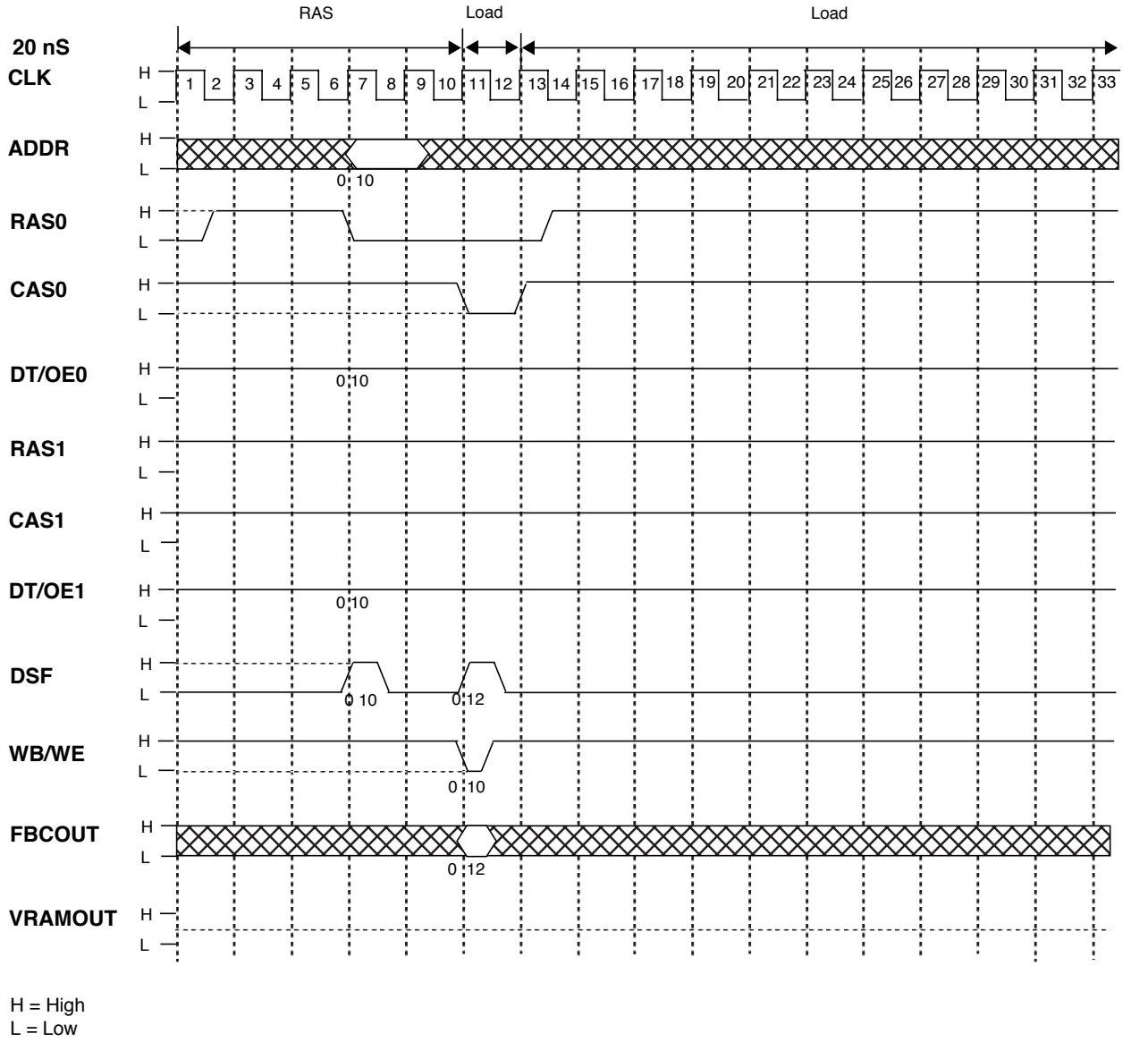


Figure 6-20 One Bank Load Color (120 nS)

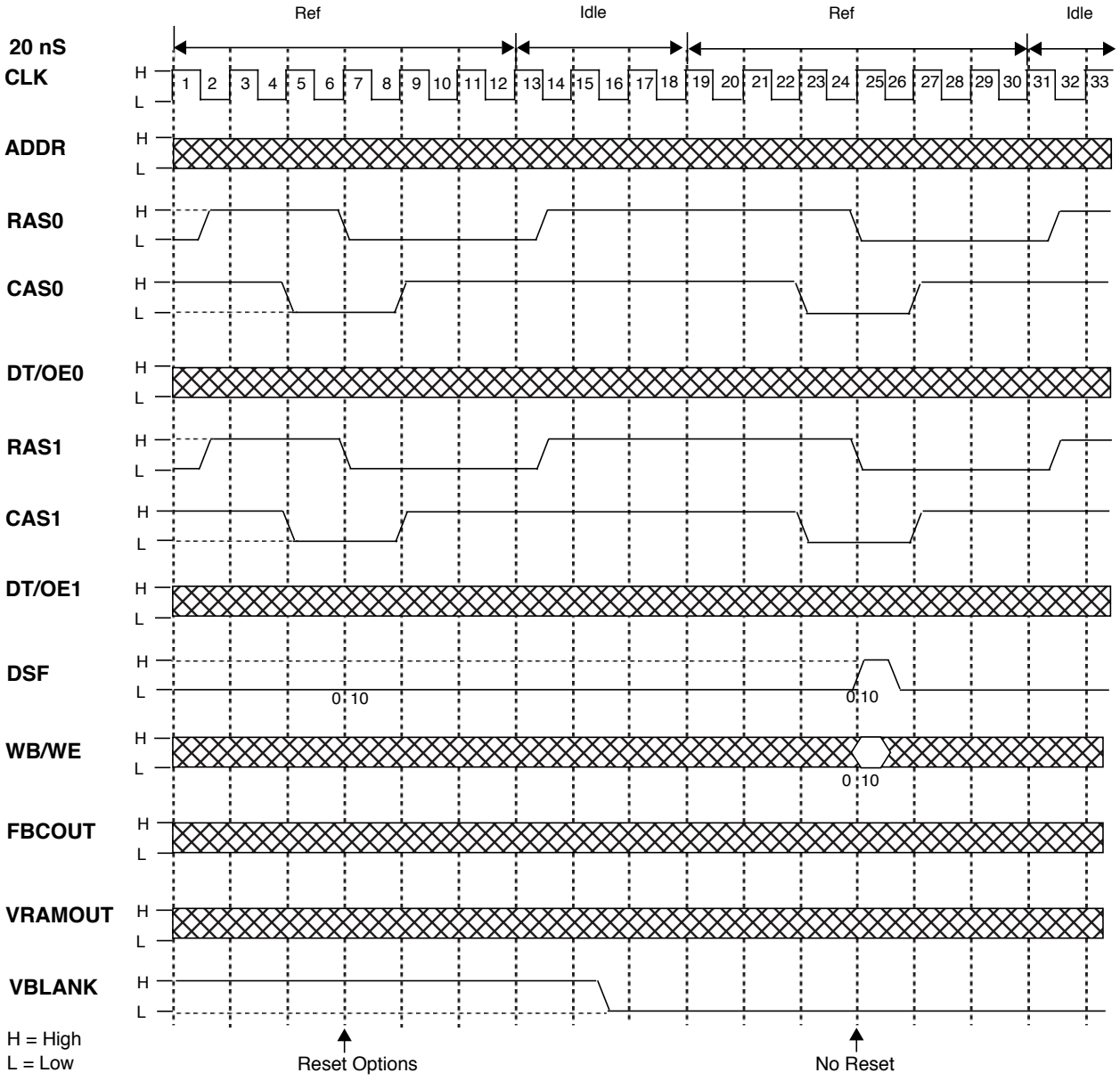


Figure 6-21 Two Bank CAS Before RAS Refresh Cycle During VBLANK and During No VBLANK (120.0 nS)

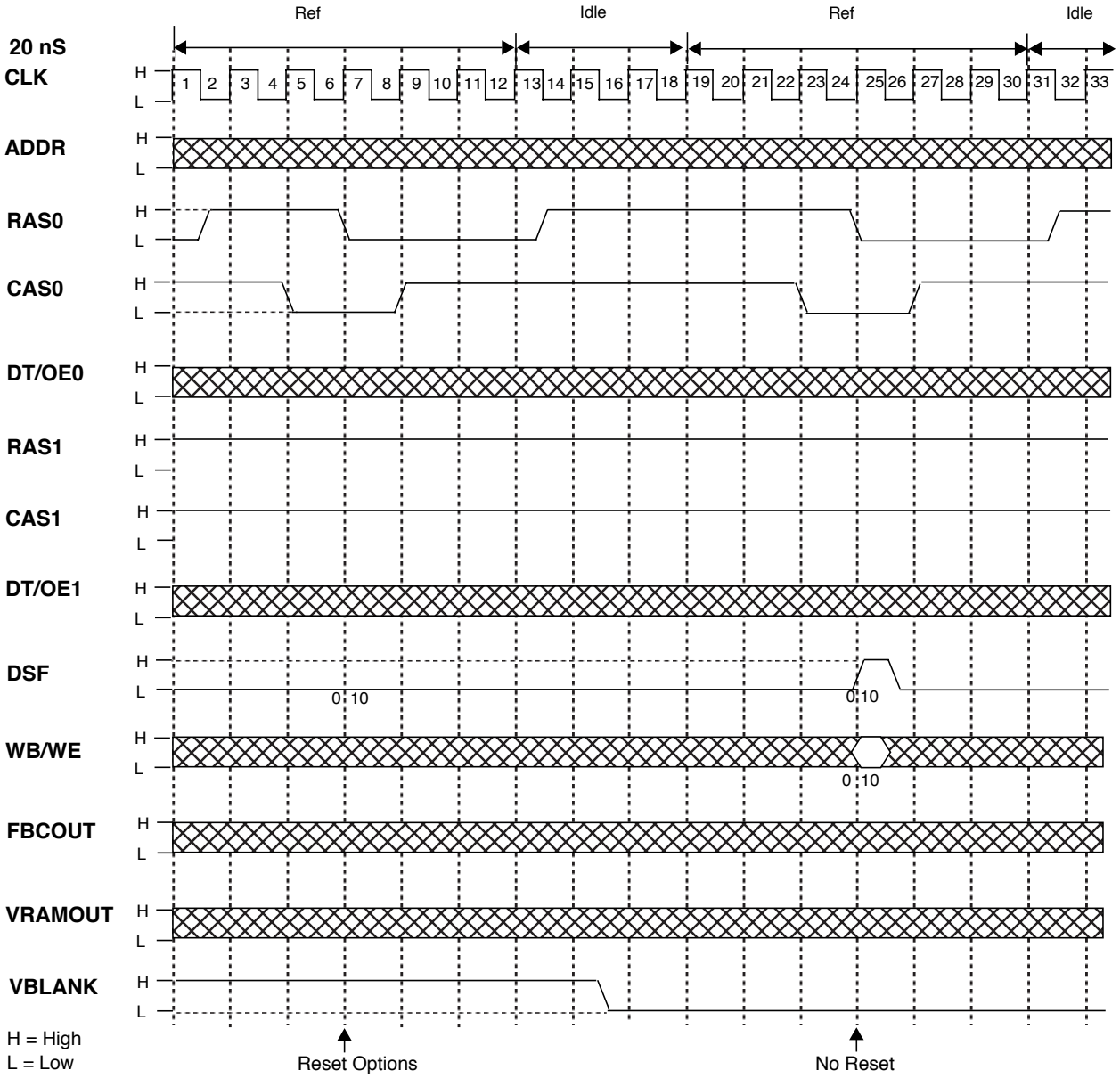


Figure 6-22 One Bank CAS Before RAS Refresh Cycle During VBLANK and During No VBLANK (120.0 nS)

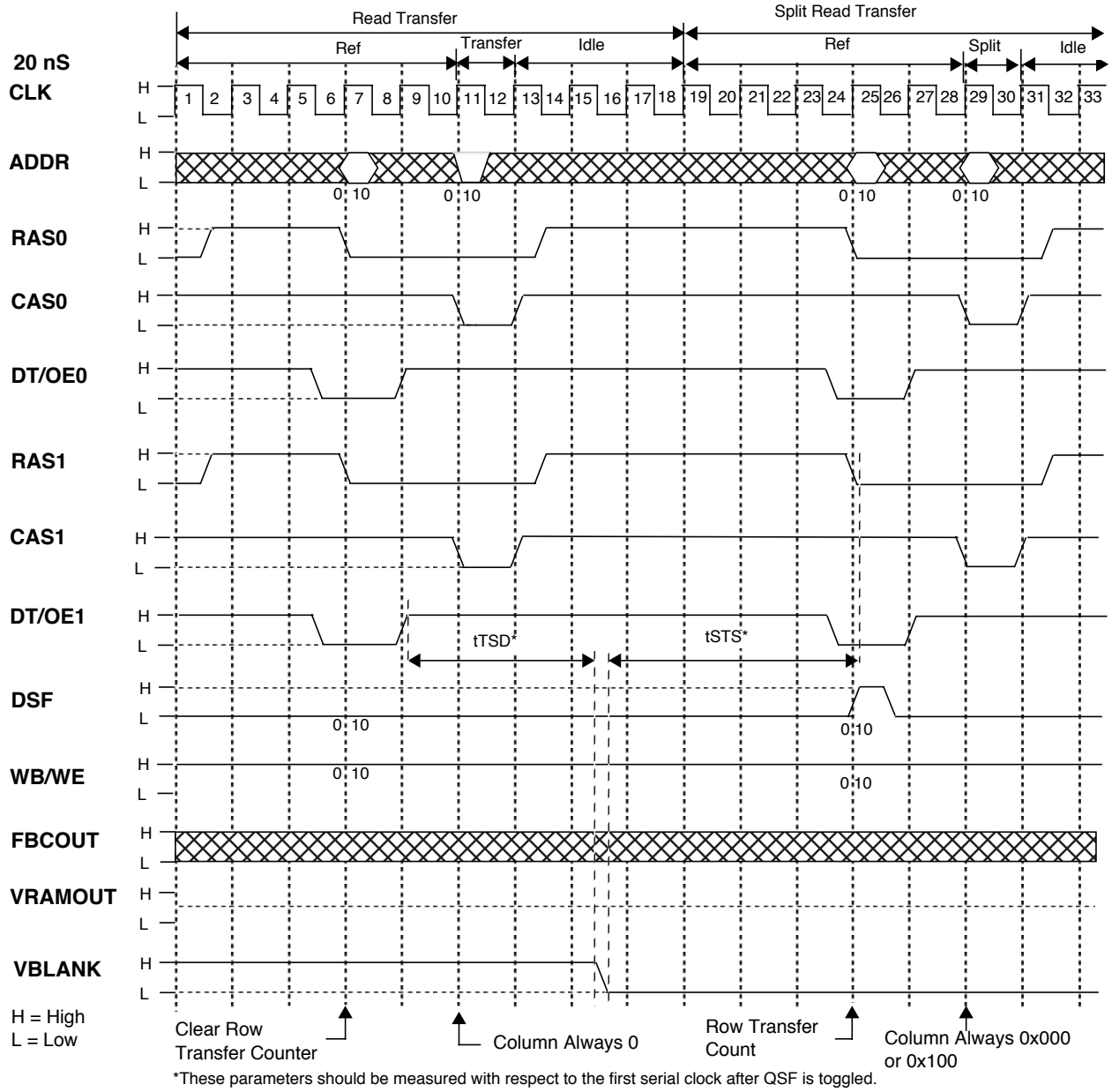


Figure 6-23 Two Bank Read Transfer During VBLANK, Two Bank Split Read Transfer During No VBLANK (120.0 nS)

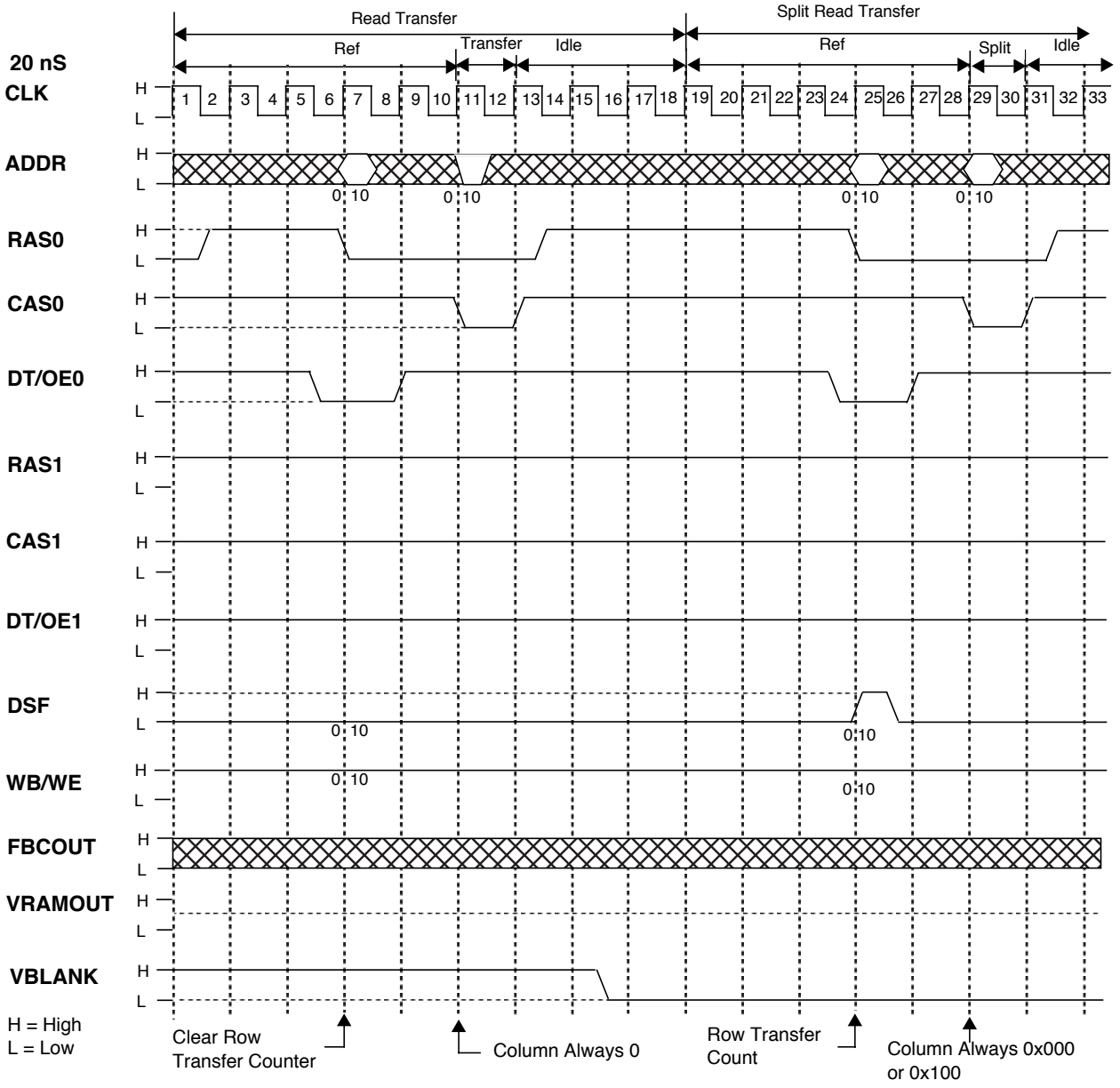


Figure 6-24 One Bank Read Transfer During VBLANK, One Bank Split Read Transfer During No VBLANK (120.0 nS)

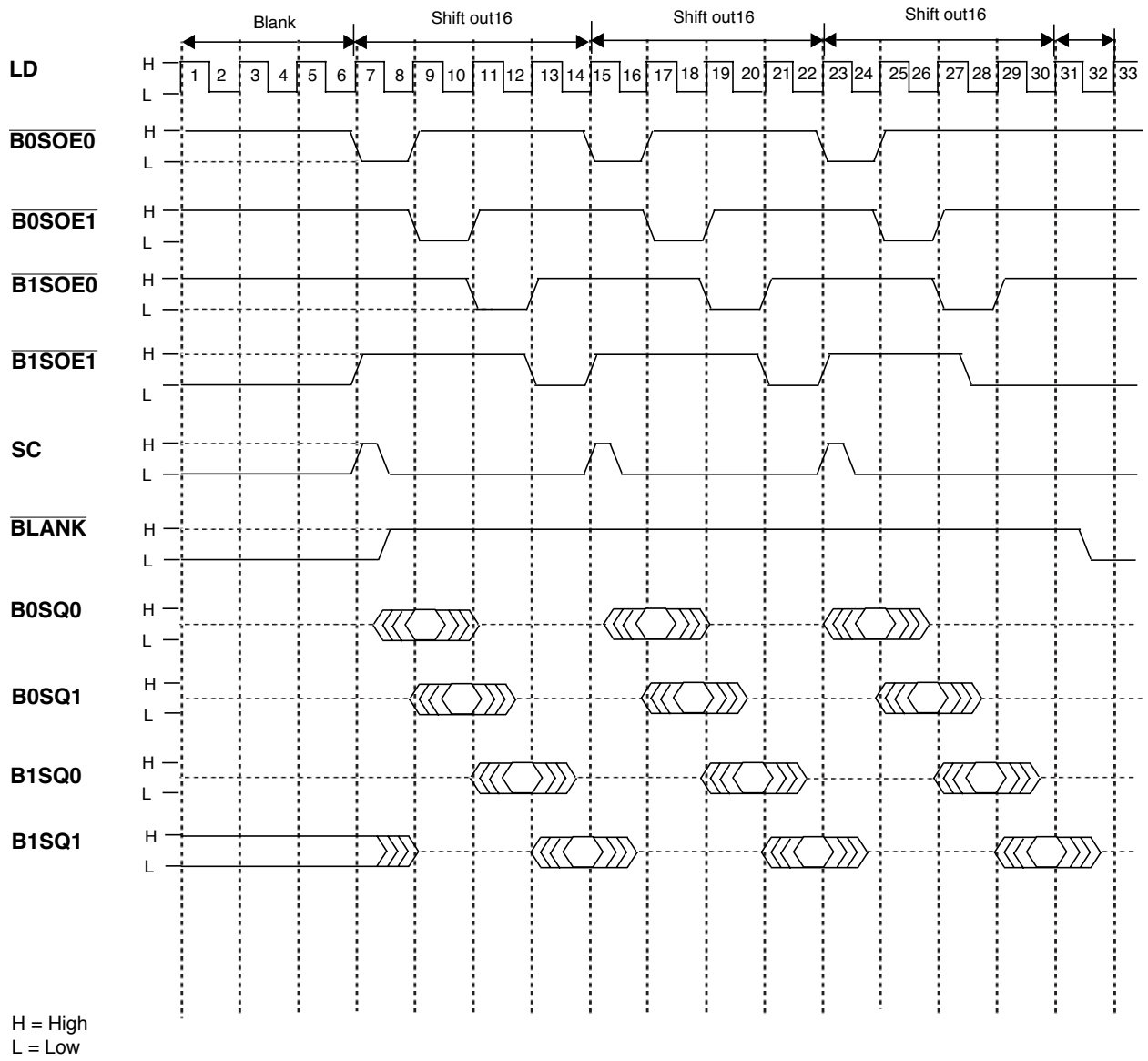


Figure 6-25 4:1 DAC Two Bank Output Control (Duplo Jr. and GXplus)

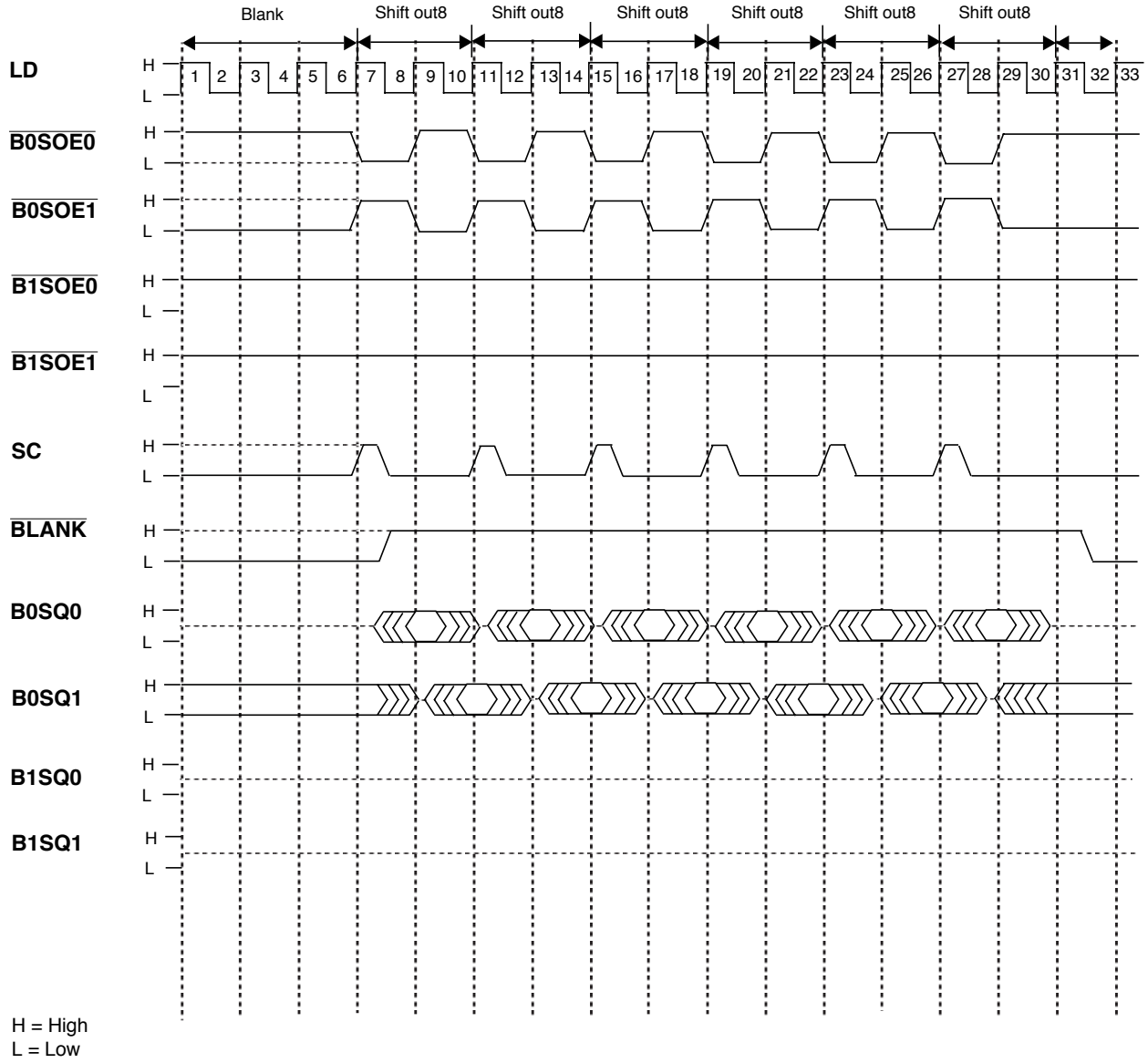


Figure 6-26 4:1 DAC One Bank Output Control (LegoSC Jr. and LegoHR Jr.)

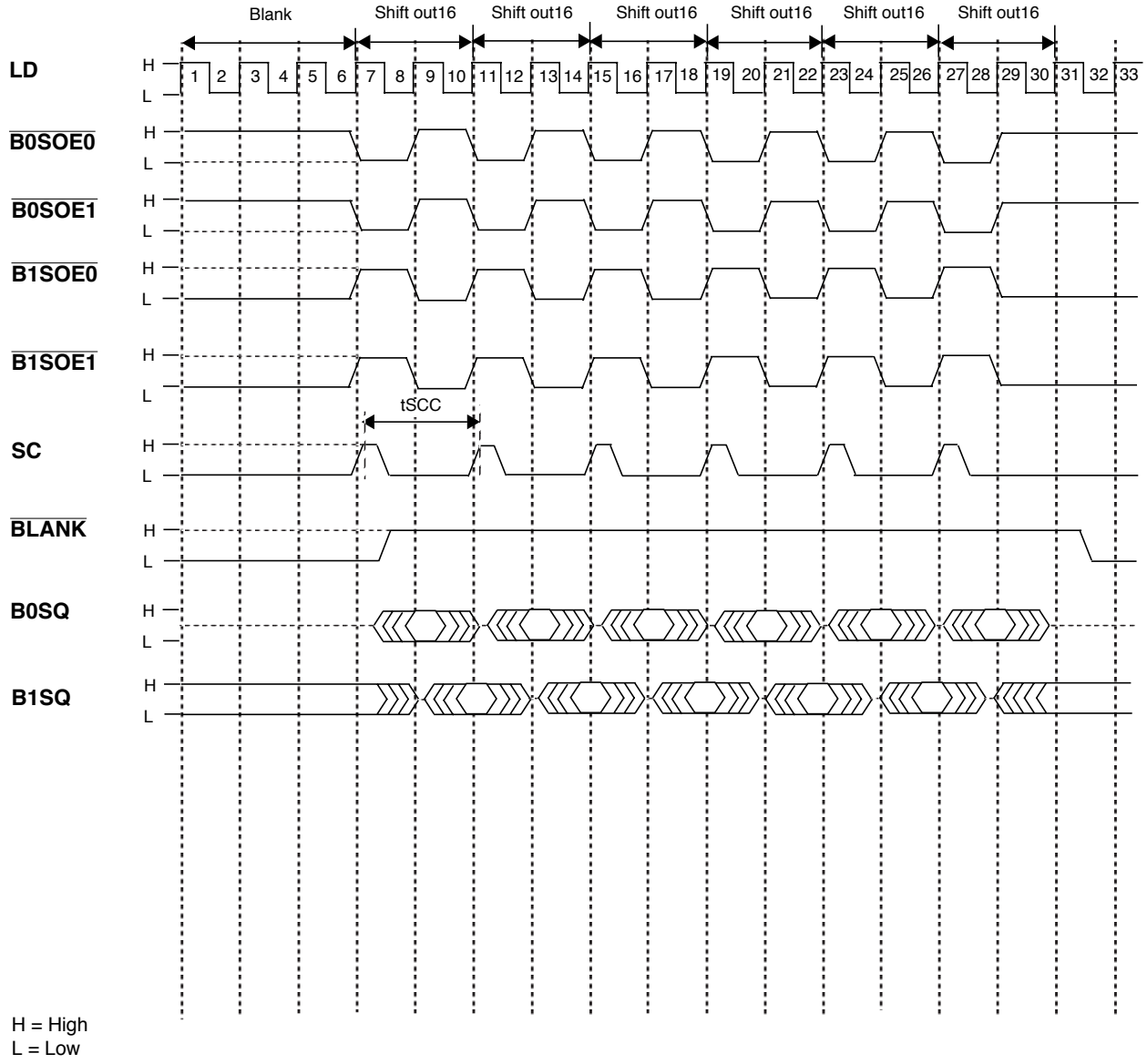


Figure 6-27 8:1 DAC Two Bank Output Control (DuploSC and TurboGX/TurboGXplus

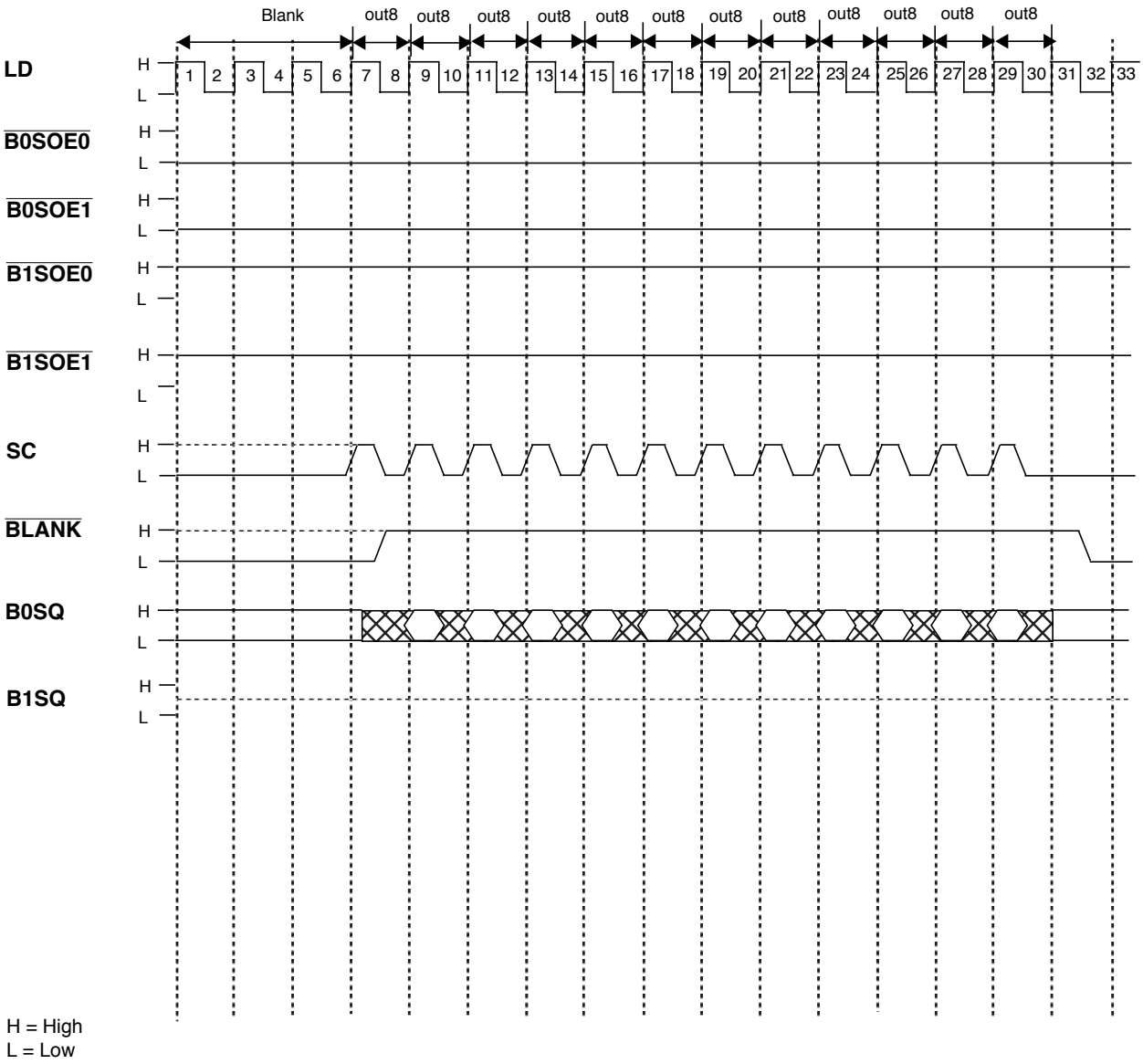


Figure 6-28 8:1 DAC One Bank Output Control (LegoSC Sr. and LegoHR Sr.)

Bt458 RAMDAC 7

This chapter describes the Bt458 RAMDAC. It provides a functional description of the chip, user accessible register information, and signal descriptions.

The Bt458 RAMDAC is used on the GX card as well as on the CPU board of the SPACRstation IPX and SPARCstation LX. The RAMDAC used on the TurboGX, and TurboGXplus cards are covered in Chapter 7.

Note – The Bt458 is used for those products (i.e., GX card) that require less than 125 MHz pixel clock and 4 pixel wide DAC. The Bt467 is used for those products (i.e., GXplus, TurboGX) that require 125 MHz or greater pixel clock, or desire an 8-pixel wide DAC. Refer to Table 8-1 for details.

7.1 Bt458 Functional Description

The Bt458 is specifically designed for high performance and high resolution color graphics. The Bt458 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. Its features include programmable blink rates, bit plane masking, blinking, color overlay capability, and a dual-port color palette RAM.

The RAMDAC Bt458 drives all three guns of a standard RS-343A color monitor. It can simultaneously display 256 colors out of an available set of 16.8 million (2^{24})colors.

Figure 7-1 shows a block diagram of the RAMDAC. It consists of an input buffer, an input multiplexer, Blink and Read Mask logic, a 256 x 24 Look-Up Table (LUT), a 4 x 24 Overlay Table, three 8-bit RS-343A compatible DACs, and CPU Interface logic. Note that only two high-speed signals are required: input clocks CLKN* and CLKP, which operate at the 92.9405 MHz (10.76 nS) pixel rate.

Four pixels are loaded into the Input Buffer from the VRAM over pixel data lines PA<7-0> through PD<7-0> on the rising edge of the 23.24 MHz (43 nS) Load Clock LDCK*. These pixels are serially read out of the Input Buffer through the four-to-one Input Multiplexer using the 92.9405 MHz pixel clock (CLKN*/CLKP). The Color Look-Up Table (LUT) maps each of the pixels in the serial pixel stream into a physical color. The three Digital-to-Analog (DAC) converters create an RS-343A compatible RGB analog output corresponding to the digital output of the LUT.

7.1.1 CPU Interface

The CPU Interface allows the CPU to access the LUT and the internal registers of the RAMDAC. The type of access is determined by Local Address lines 2 and 3 as follows:

LA3	LA2	Type of Access
0	0	Address Register (AR7–AR0)
0	1	Look-Up Table
1	0	Control Registers
1	1	Overlay Registers

Two internal counters allow fast access to the LUT and the Overlay Registers:

- An 8-bit address register (AR0–AR7) generates addresses for the Color Memory locations and the Control Registers. This register increments at the end of each third (blue) access when LA2 = 1. Thus the CPU does not have to rewrite the Address Register with consecutive values thereby saving CPU time and bus bandwidth for transfers to or from consecutive Color Memory locations. It operates as described below.

AR7–AR0	LA3	LA2	Location or Register Addresses
0x00-0xFF	0	1	Color LUT location 00 through FF
0x00	1	1	Overlay Register 0
0x01	1	1	Overlay Register 1
0x02	1	1	Overlay Register 2
0x03	1	1	Overlay Register 3
0x04	1	0	Read Mask Register
0x05	1	0	Blink Mask Register
0x06	1	0	Command Register
0x07	1	0	Test Register

- A modulo 3 Counter (ARb, ARa) controls which byte of the 24-bit Color Memory word is accessed. This register is not accessible by the CPU. It increments at the end of each CPU access with LA2 = 1 (color operations) and is reset to 0 at the end of each CPU access with LA2 = 0 (Control Registers operations). It operates as follows:

ARb	ARa	Color Byte Being Accessed
0	0	Red
0	1	Green
1	0	Blue

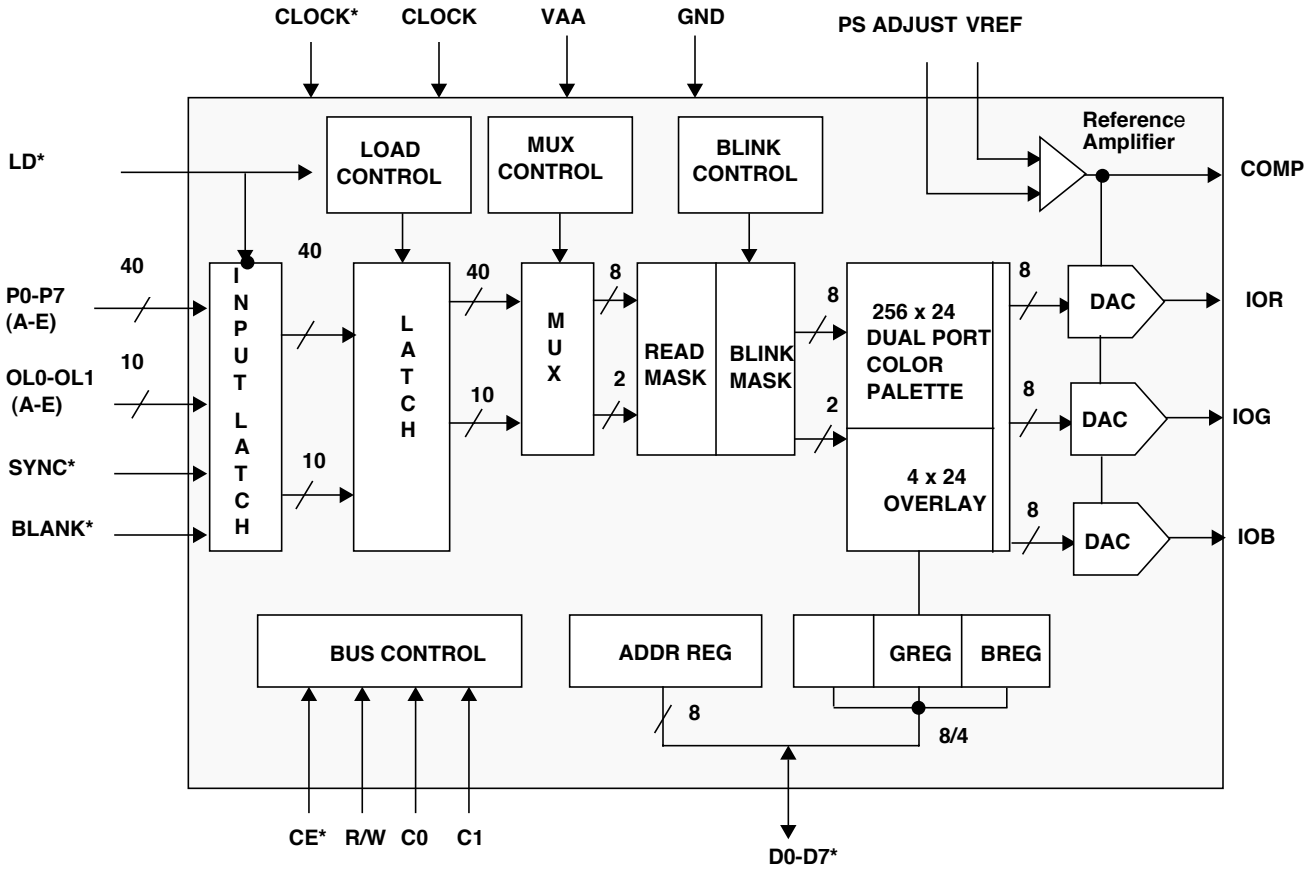


Figure 7-1 Bt458 Functional Block Diagram

7.1.2 VRAM Interface

The RAMDAC accepts data from the VRAM at one fourth the rate that it presents RGB data to the monitor. This is done using the Input Buffer and the four-to-one Input Multiplexer.

The rising edge of the 23.24 MHz LDCK* clock loads the following signals into the Input Buffer:

- Pixel data inputs (PA<7..0> through PD<7..0>) from the VRAM.
- The eight overlay data inputs (OL0<A..D> and OL1<A..D>) from the TEC section of the chip.
- The BLANK* signal from the LSC chip, and the SYNC* signal, which is grounded.

The 92.9405 MHz pixel clock (CLKN*/CLKP) gates each of the four pixel bytes out of the Input Multiplexer in serial thus providing a four-to-one multiplexing of the pixel bytes. The frequency of the pixel clock is four times that of the load clock. The multiplexer first outputs the pixel from PA<7..0>, then PB, PC, and PD. It then repeats this cycle with the next four bytes loaded from the VRAM.

Note that the eight overlay data signals are also multiplexed four-to-one. The multiplexer thus outputs OL0A and OL1A, then OLxB, OLxC, and OLxD.

Table 7-1 shows each of the possible read and write access modes.

Table 7-1 Truth Table for Bt458 Read and Write Operations

R/W	C1	C0	ADDR1	ADDR0	Function
0	0	0	x	x	Write Address Register; D0-D7 → ADDR2-9, 0 → ADDR0-1
0	0	1	0	0	Write Red Color; D0-D7 → RREG, increment ADDR0-9
0	0	1	0	1	Write Green Color; D0-D → GREG, increment ADDR0-9
0	0	1	1	0	Write Blue Color; D0-D → BREG, write color palette RAM, increment ADDR0-9
0	1	0	x	x	Write Control Register; D0-D7 → reg(ADDR), 0 → ADDR0-1
0	1	1	0	0	Write Red Color;D0-D → RREG, increment ADDR0-9
0	1	1	0	1	Write Green Color; D0-D → GREG, increment ADDR0-9
0	1	1	1	0	Write Blue Color; D0-D → BREG, write overlay register, increment ADDR0-9
1	0	0	x	x	Read Address Register; ADDR2-9 → D0-D7,0 → ADDR0-1
1	0	1	0	0	Read Color Palette Red; R0-R7 → D0-D7, increment ADDR0-9
1	0	1	0	1	Read Color Palette Green; G0-G7 → D0-D7, increment ADDR0-9
1	0	1	1	0	Read Color Palette Blue; B0-B7 → D0-D7, increment ADDR0-9
1	1	0	x	x	Read Control Register; reg(ADDR)→ D0-D7, 0 → ADDR0-1
1	1	1	0	0	Read Overlay Palette Red; R0-R7→ D0-D7, increment ADDR0-9
1	1	1	0	1	Read Overlay Palette Green;G0-G7→ D0-D7, increment ADDR0-9
1	1	1	1	0	Read Overlay Palette Blue;B0-B7→ D0-D7, increment ADDR0-9

Key:

→ = gets the value of

RREG = Red Byte Register

GREG = Green Byte Register

BREG = Blue Byte Register

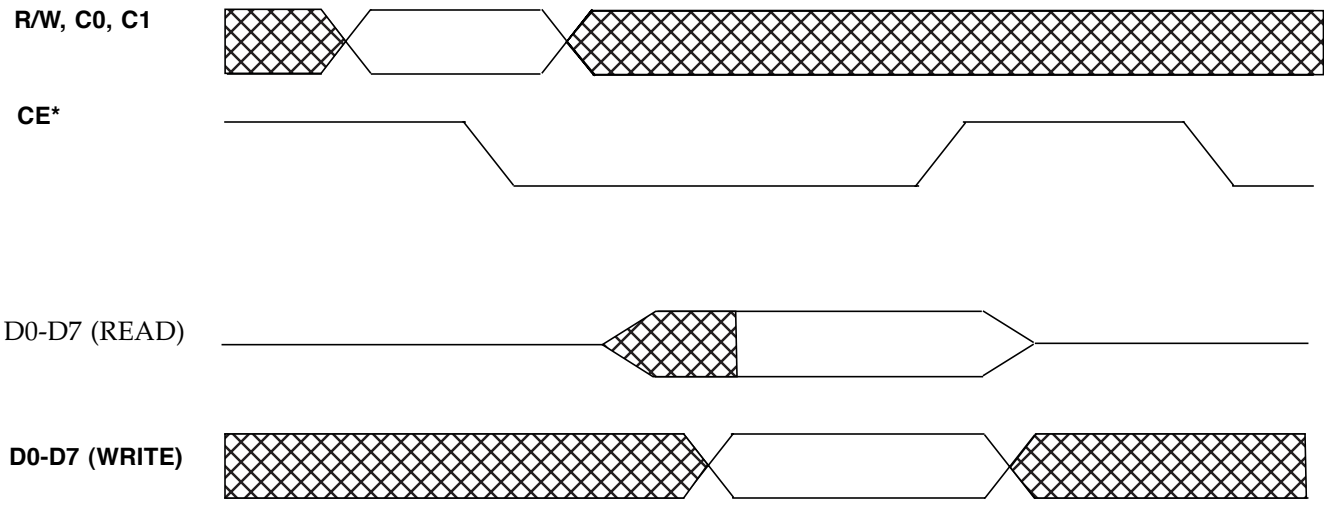


Figure 7-2 Host MPU Read/Write Timing

7.1.3 *Frame Buffer Interface*

To enable pixel data to be transferred to/from the RAMDAC at reasonable data rate (up to 32 MHz), the Bt458 uses internal latches and multiplexers. As illustrated in Figure 7-3. On the rising edge of LD* and sync and blank, color and overlay for either four or five consecutive pixels are latched into the device via the 40-pixel select inputs. These inputs are (P0–P7 {A-E}) and the sync*, and blank inputs. The sync and blank timing is recognized only with four or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

7.1.4 *Internal Multiplexing*

The LD* signal may be phase shifted, in any amount, relative to CLOCK to simplify the frame buffer interface timing. It enables the LD* signal to be derived externally, dividing the CLOCK by four or five. This should be

independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of CLOCK phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD signal by at least one, but not more than four clock cycles. This load signal transfers the latched pixel and overlay data into a second set of latches which are then internally multiplexed at the CLOCK rate (up to 125 MHz).

Since 4:1 multiplexing is specified, only one rising edge of LD* should occur every four CLOCK cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

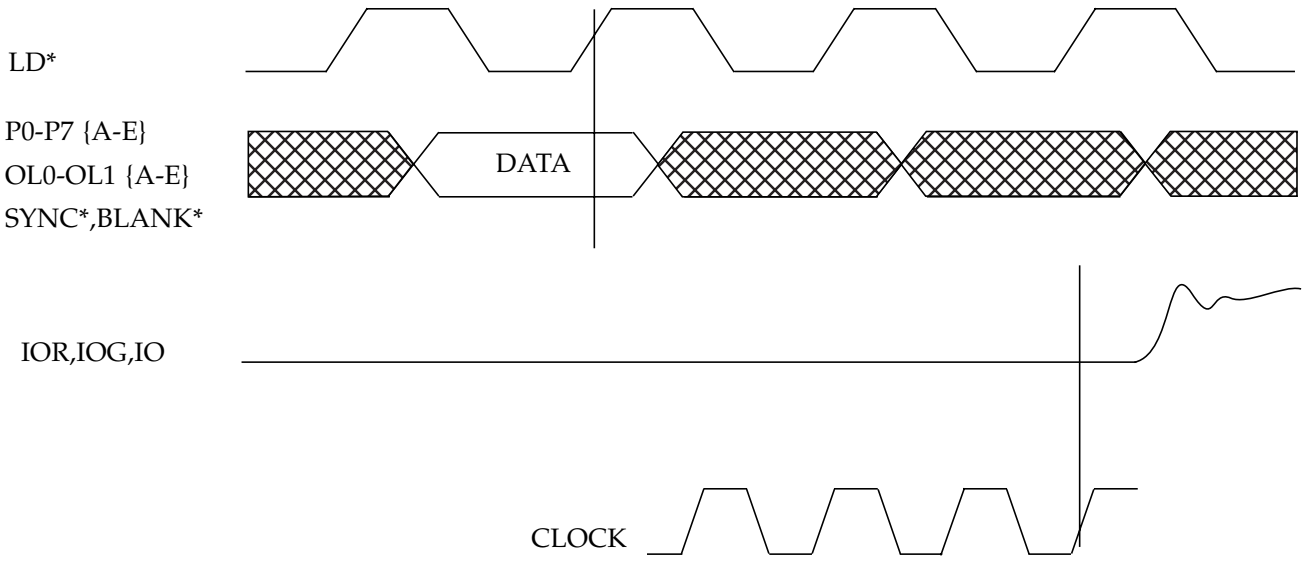


Figure 7-3 Video Input/Output Timing

7.1.5 Video Side Timing

The following figures show video side timing diagrams:

Figure 7-4 Horizontal sync and blanking cycle

Figure 7-5 Vertical sync and blanking cycle

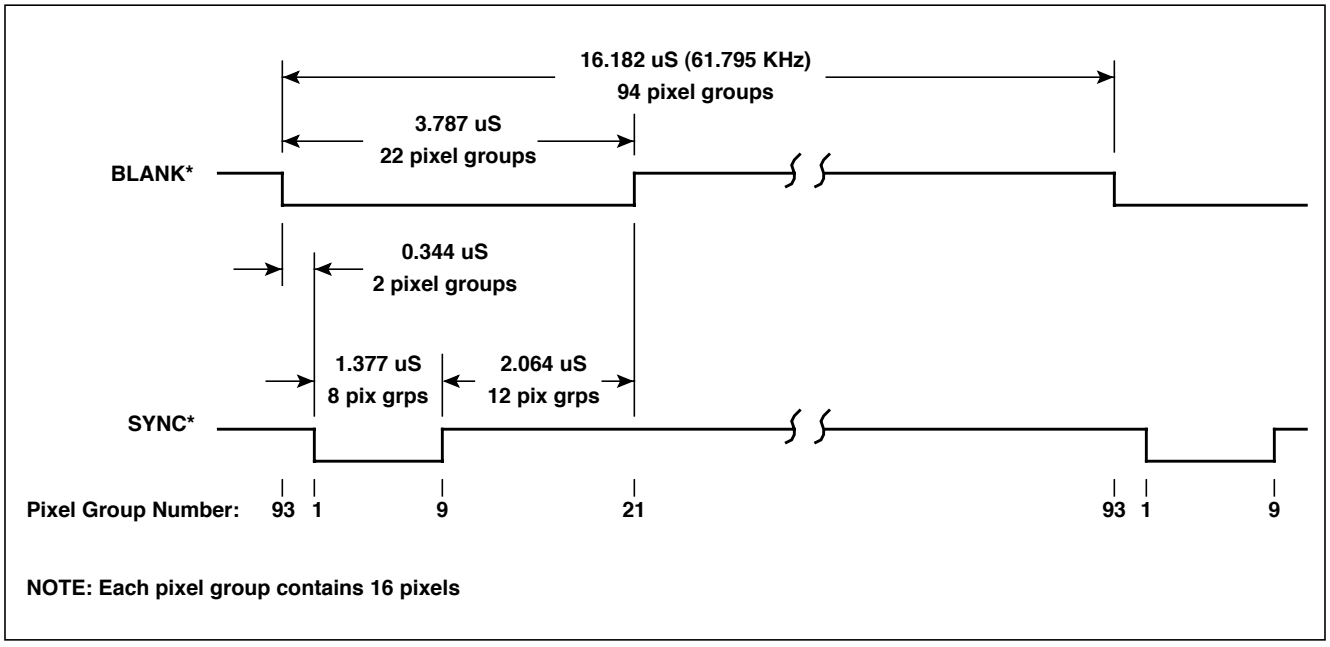


Figure 7-4 Horizontal Sync and Blanking Cycle

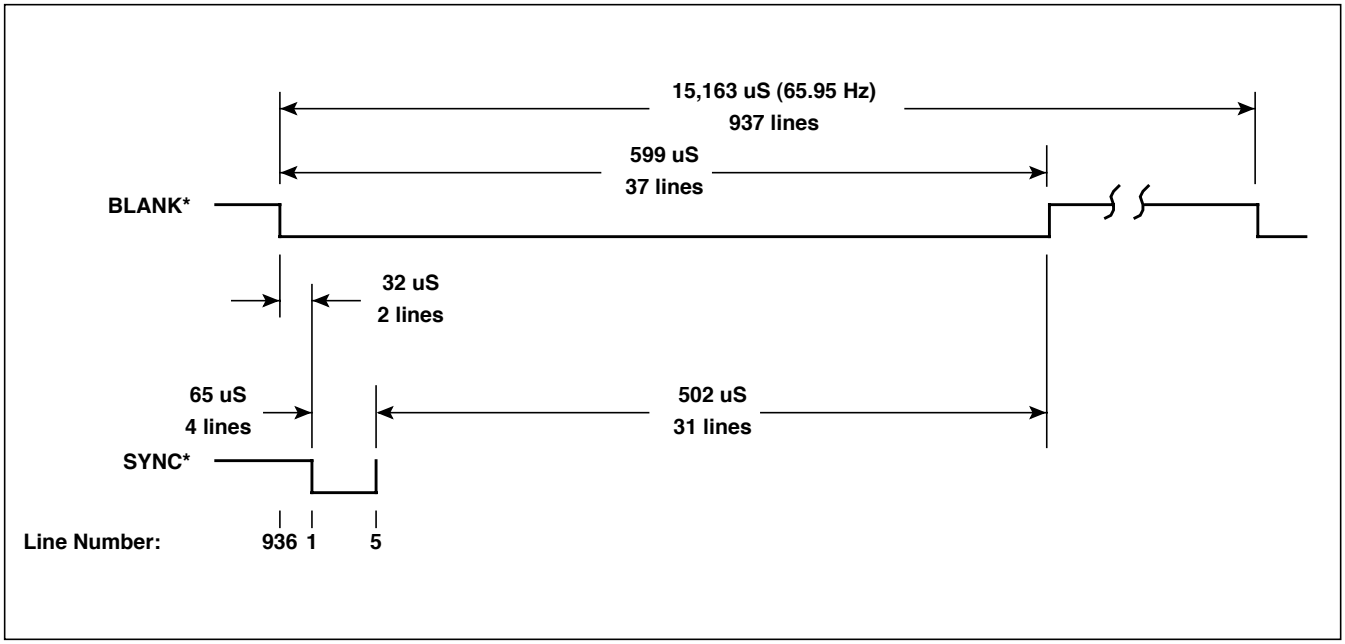


Figure 7-5 Vertical Sync and Blanking Cycle

7.1.6 Color Selection

The eight pixel data bits and two overlay bits, gated out of the multiplexer during each pixel clock cycle, are processed by the Blink and Read Mask, and by the Command Register. This information is then used to select an entry in the Color LUT or an Overlay Register to provide color information.

The 8-bit Read Mask Register selectively enables or disables bit planes from being presented to the Color LUT. The 8-bit Blink Mask Register selectively enables or disables blinking on a bit plane. Bit 4 and 5 of the Command Register determine the blink-rate duty cycle. The counter that generates the internal blink clock is incremented during the vertical retrace intervals. These intervals are detected when BLANK* is low for a period of at least 256 load clock cycles.

On the rising edge of the CLOCK cycle, eight bits of color information (P0 - P7) and two bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

Note, P0 is the LSB when addressing the color palette RAM. Table 7-2 shows the truth table used for color selection.

Table 7-2 Palette and Overlay Select Truth Table

CR6	OL1	OL0	P7 - P0	Palette Entry Addressed
1	0	0	$00	Color palette entry $00
1	0	0	$01	Color palette entry $01
:	:	:	:	:
1	0	0	$FF	Color palette entry $FF
0	0	0	$XX	Overlay color 0
X	0	1	$XX	Overlay color 1
X	1	0	$XX	Overlay color 2
X	1	1	$XX	Overlay color 3

7.1.7 *Overlay Color Selection*

The four 24-bit Overlay Registers provide four different overlay colors that are selected by the two overlay bits. Bits 0 and 1 of the Command Register act as a read mask, and bits 2 and 3 act as a blink mask on the overlay inputs. Thus an overlay output (OVLADDR0 or OVLADDR1) is present only when the corresponding read mask bit and blink mask bit are true. When the blink mask is enabled, an internal blink clock turns the overlay output off and then on.

The Overlay Register is selected as shown below. Note that when OVLADDR1 = 0 and OVLADDR0 = 0, bit 6 of the Command Register selects between Overlay Register 0 and the Look-Up Table output addressed by the eight pixel bits.

OVLADDR1	VLADDR0	Bit 6 = 0	Bit 6 = 1
0	0	Overlay Register 0	LUT
0	1	Overlay Register 1	Overlay Register 1
1	0	Overlay Register 2	Overlay Register 2
1	1	Overlay Register 3	Overlay Register 3

7.1.8 Overlay Select Input Lines

The OL0-OL1 {A-E} overlay select inputs (TTL compatible) are latched on the rising edge of LD*. They, in conjunction with bit 6 of the command register, specify which palette is to be used for color information. See Table 7-3 below for details.

Table 7-3 Signals Between RAMDAC Chip and the TEC Block

OL1	OL0	CR6 = 1
0	0	Color Pallette RAM
0	1	Overlay Color 1
1	0	Overlay Color 2
1	1	Overlay Color 3

7.1.9 Video Generation

During each pixel clock cycle, 24 bits of information from either the LUT or an Overlay Register are sent to the three 8-bit DACs. These DACs convert the color memory digital output into RGB RS-343A analog signals for the red, green, and blue guns of the monitor.

The SYNC* and BLANK* signals are routed to the DACs through a pipeline delay circuit that delays these signals the same amount that the video stream is delayed. The BLANK* signal goes to all three DACs and the SYNC* signal only goes to the Green DAC.

The output levels of the DACs are shown in Figure 6-6 and Figure 7-7.

IOR, IOG, IOB	
MA	V
19.05	0.714
0.00	0.000

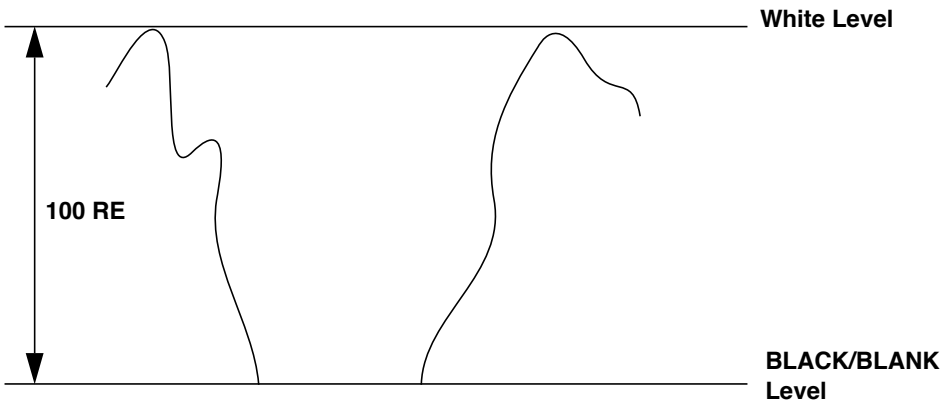


Figure 7-6 DAC Current and Voltage Output Levels (zero offset, 76 Hz monitors)

IOR, IOG, IOB	
MA	V
19.05	0.714
1.44	0.054

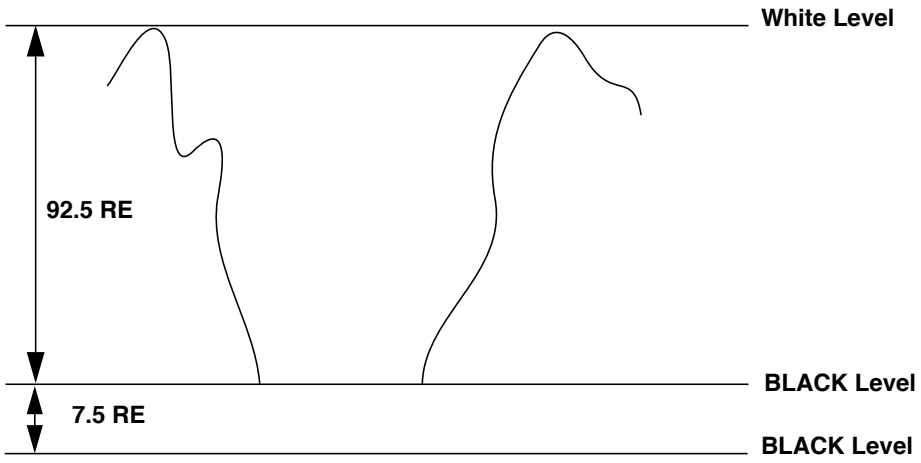


Figure 7-7 DAC Current and Voltage Output Levels (pedestal offset, 66Hz monitors)

7.1.10 Signal Descriptions

The input and output signals of the RAMDAC chip are described in Table 7-4 and Table 7-5. Also see Table 7-6 for Bt458 pin list. Note that the I/O column indicates the signal input or output direction from the RAMDAC chip's point of view. Also note that the signal names in these tables are the names used on the GX card schematic diagram.

Table 7-4 Signals Between RAMDAC Chip and the LSC Chip

Name	Pin	I/O	Description
BLANK*	59	I	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored. It overrides the color pixel and overlay data to force the RED, GREEN, and BLUE video output signals to their blanking levels. Blanking is required during the monitor's vertical and horizontal retrace period.
CS_DAC*	20	I	Chip Select signal that enables the CPU Interface logic. Data on the Local Data bus LD<31.. 24> is internally latched on the rising edge of CS_DAC* during write operations.
LD*	60	I	Load control input (TTL compatible). The P0-P7 {A-E}, OL0-OL1 {A-E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. This signal is one-fourth the rate of the pixel clock frequency.

Table 7-5 Bt458 Pin Descriptions

Pin Name	Pin Numb	I/O	Description
BLANK*	59	I	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	58	I	Composite sync control input (TTL compatible). A logical zero on this input switches off a current source on the IOG output. SYNC* does not override any other control or data input. It should be asserted only during the blanking interval. It is latched on the rising edge of LDCK*.
LD*	60	I	Load control input (TTL compatible). The P0-P7 {A-H}, OL0-OL1 {A-H}, BLANK*, and SYNC* inputs are latched on the rising edge of the LD*. This signal is one-fourth the rate of the pixel clock frequency. LD*, while it is either 1/4 or 1/5 the CLOCK rate, may be phase independent of the CLOCK and CLOCK* inputs.
P0-P7 ({A-H)	6-11	I	Overlay select input (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. Either four or five consecutive pixels (up to eight bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused pixel inputs must be connected to the regular PCB ground plane. Note, that the {A} pixel is output first, followed by the {B} pixel, etc., until all four or five pixels have been output. Then the cycle repeats.
Ol0-OL1 {A-**H)**	11-8, 6-3		Overlay select input (TTL compatible). These control inputs are latched on the rising edge of LD*, and in conjunction with bit 6 of the command register, specify which palette is to be used for color information as shown below:

OL1	OL0	CR6 = 1	CR6 = 0
0	0	Color Pallette RAM	Overlay Color 0
0	1	Overlay Color 1	Overlay color 1
1	0	Overlay Color 2	Overlay color 2
1	1	Overlay Color 3	Overlay color 3

When accessing the overlay palette, the P0-P7 {A-H} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for eight consecutive pixels are input through this port. Unused inputs should be connected to GND.

R, G, B	28, 29, 30	O	Red, green, and blue video current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable.
AGND (GND)	21, 22, 34, 36, 35		Analog ground.
VAA	23, 27, 35, 37, 63, 64	PG	Analog power.

Pin Name	Pin Numb	I/O	Description
COMP	32	PG	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 *u*F ceramic capacitor must be connected between this pin and VAA.
FS ADJUST	31	I	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal. Using the oscilloscope, the voltage at this pin should be approximately equal to the voltage at the VREF pin. The relationship between RSET and the full scale output current on IOG is: RSET (ohms) = 10,684* VREF (V)/IOG (mA) The full scale output current on IOR and IOB for a given RSET is: IOR, IOG, IOB, (mA) = 7,457 * VREF (V) / RSET (ohms)
VREF	33	I	Voltage reference input. An external reference circuit must supply this input with a 1.235V (typical) reference. A 0.01 *u*F ceramic capacitor must be used to decouple this input to VAA. The use of a resistor network to generate the reference is not recommended as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs.
CLK, CLK*	62, 61	I	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	20	I	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operation, data is internally latched on the rising edge of the CE*.
R/W	26	I	Read/Write control input. To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, the CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	24, 24	I	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed. They are latched on the falling edge of CE*.
D0-D7	12-19		Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.

Table 7-6 Bt 458 Pin List

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	59	P5A	52	VAA	23
SYNC*	58	P5B	51	VAA	27
LD*	60	P5C	50	VAA	35
CLOCK	62	P5D	49	VAA	37
CLOCK*	61	P5E	48	VAA	63
0A	1	P6A	47	VAA	64
P0B	84	P6B	46	AGND	21
P0C	83	P6C	45	AGND	22
P0D	82	P6D	44	AGND	34
P0E	81	P6E	43	AGND	36
P1A	80	P7A	42	AGND	65
P1B	79	P7B	41	COMP	32
P1C	78	P7C	40	FS ADJUST	31
PID	77	P7D	39	VREF	33
P1E	76	P7E	38	CE*	20
P2A	75	OL0A	11	R/W	26
P2B	74	OL0C	10	C1	25
P2C	73	OL0C	9	D0	24
P2D	72	OL0D	8	D0	12
P2E	71	OL0E	7	D1	13
P3A	70	OL1A	a6	D2	14
P3B	69	OL1B	5	D3	15
P3C	68	OL1C	4	D4	16
P3D	67	OL1D	3	D5	17
P3E	66	OL1E	2	D6	18
P4A	57	IOR	28	D7	19
P4B	56	IOG	29	P4C	55
IOB	30	P4D	54	P4E	53

7.2 Programming the RAMDAC

The user can access and program the following registers: Address, Command, Read Mask, Blink Mask, and Test.

7.2.1 Address Register

The Address Register is accessed when LA3 and LA2 are 0. If LWRITE* is low, local data bus lines LD<31..24> are loaded into the Address Register. If LWRITE* is high, the contents of the Address Register are loaded onto local data bus lines LD<31..24>.

7.2.2 Command Register

The Command Register is an 8-bit register located at address 0x06. Table 7-7 describes this register.

7.2.3 Read Mask Register

The Read Mask Register is an 8-bit register located at address 0x04. It enables (logical 1) or disables (logical 0) pixel bit planes from addressing the Color LUT. Bit 0 masks inputs PA<0> through PD<0>, bit 1 masks inputs PA<1> through PD<1>, and so on. Overlay plane masking is controlled by bits 1 and 0 of the Command Resister as shown in Table 7-7.

7.2.4 Blink Mask Register

The Blink Mask Register is an 8-bit register located at address 0x05. It enables (logical 1) or disables (logical 0) pixel bit planes from blinking. Bit 0 masks inputs PA<0> through PD<0>, bit 1 masks inputs PA<1> through PD<1>, and so on. When enabled, the bit plane toggles between its original value and logical 0 at the selected rate and duty cycle. Overlay plane masking is controlled by bits 3 and 2 of the Command Resister as shown in Table 7-7.

7.2.5 Test Register

The Test Register is an 8-bit register located at address 0x07. It can read back data presented to the DACs from the Color Memory (either pixel or overlay data). Bits 7 through 4 contain color information and bits 3 through 0 contain control information as described below.

Test Register Bit	Function	
D7–D4	Color nibble (4 bits of red, green, or blue)	
3	0 = Select high nibble	1 = Select low nibble
2	0 = Disable blue data	1 = Enable blue data
1	0 = Disable green data	1 = Enable green data
0	0 = Disable red data	1 = Enable red data

Bits D7 through D4 are defined only when exactly one of the bits 2 through 0 is a logical 1. When unused, this register should be initialized to 0x00.

Table 7-7 Command Register Definition

Bit	Name	Definition	Description
CR7	Multiplex Select	0 = 4:1 Multiplexing 1 = 5:1 Multiplexing	Specifies 4:1 or 5:1multiplexing for pixel and overlay data. For the GX card, this bit is set to 0 for 4:1 multiplexing.
CR6	RAM Enable	0 = Use Overlay Color 0 1 = Use Color Palette RAM	When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information. Set to 1.
CR5, CR4	Blink Rate Selection	00 = 1.024 Seconds (75/25) 01 = 0.512 Seconds (50/50) 10 = 1.024 Seconds (50/50) 11 = 2.048 Seconds (50/50)	Specify the blink rate cycle time and duty cycle of the internal blink clock assuming a 60 Hz noninterlaced or 30 z interlaced refresh rate. For applications having other refresh rates, i.e., 57 Hz noninterlaced, the blink rate is determined by scaling the specified values (i.e., multiplying by 57/60). The numbers in parentheses specify the duty cycle (% on/off). Set to 00.
CR3	OL1 Blink Enable	0 = Disable Blinking 1 = Enable Blinking	When set to 1, this bit forces the OL1 {A-E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL1 {A-H} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one. Set to 0.
CR2	OL0 Blink Enable	0 = Disable Blinking 1 = Enable Blinking	When set to 1, this bit forces the OL0 {A-E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL0 {A-E} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one. Set to 0.
CR1	OL1 Display Enable	0 = Disable 1 = Enable	When set to 0, this bit forces the OL1{A-E} inputs to a logical 0 before selecting the palettes. When set to 1, it does not affect the value of the OL1 {A-E} inputs. Set to 1.
CR0	OL0 Display Enable	0 = Disable 1 = Enable	When set to 0, this bit forces the OL0{A-E} inputs to a logical 0 before selecting the palettes. When set to 1, it does not affect the value of the OL0 {A-E} inputs. Set to 1.

Bt467 RAMDAC 8

This chapter describes the Bt467 RAMDAC and its implementation on the Single Chip GX card. It provides a functional description of the chip, user accessible register information, and signal descriptions.

The Bt467 RAMDAC is currently used on the GXplus, TurboGXplus, and TurboGX cards.

Note – The Bt458 RAMDAC is used for those products (i.e., GX card) that require less than 125 MHz pixel clock and 4 pixel wide DAC. The Bt467 RAMDAC is used for those products (i.e., GXplus, TurboGX, and TurboGXplus) that require 125 MHz or greater pixel clock, or desire an 8-pixel wide DAC. Refer to Table 8-1 for details.

8.1 Bt467 Functional Description

The Bt467 RAMDAC is specifically designed for high performance and high resolution color graphics. The Bt467 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. Its features include programmable blink rates, bit plane masking, blinking, color overlay capability, and a dual-port color palette RAM. The Bt467 is register compatible with the Bt458. Its architecture enables the display of 1600x1280 pixel bit mapped color graphics (8 bits per pixel plus 2 bits of overlay information).

The Bt467 RAMDAC drives all three guns of a standard RS-343A color monitor. It can simultaneously display 256 colors out of an available set of 16.8 million (2^{24}) colors. It generates RS-343A compatible red, green, and blue and is capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering.

Figure 8-1 shows a functional block diagram of the RAMDAC. It consists of an input buffer, an input multiplexer, Blink and Read Mask logic, a 256 x 24 Look-Up Table (LUT), a 4 x 24 Overlay Table, three 8-bit RS-343A compatible DACs, and CPU Interface logic. Note that only two high-speed signals are required: input clocks CLKN* and CLKP, which operate at the 92.9405 MHz (10.76 nS) to 227 MHz (4.41 nS) pixel rate.

Eight pixels are loaded into the Input Buffer from the VRAM over pixel data lines PA<7..0> through PD<7..0> on the rising edge of the 23.24 MHz (43 nS) Load Clock LDCK*. These pixels are serially read out of the Input Buffer through the four-to-one Input Multiplexer using the 92.9405 MHz pixel clock (CLKN*/CLKP). The Color Look-Up Table (LUT) maps each of the pixels in the serial pixel stream into a physical color. The three Digital-to-Analog (DAC) converters create an RS-343A compatible RGB analog output corresponding to the digital output of the LUT.

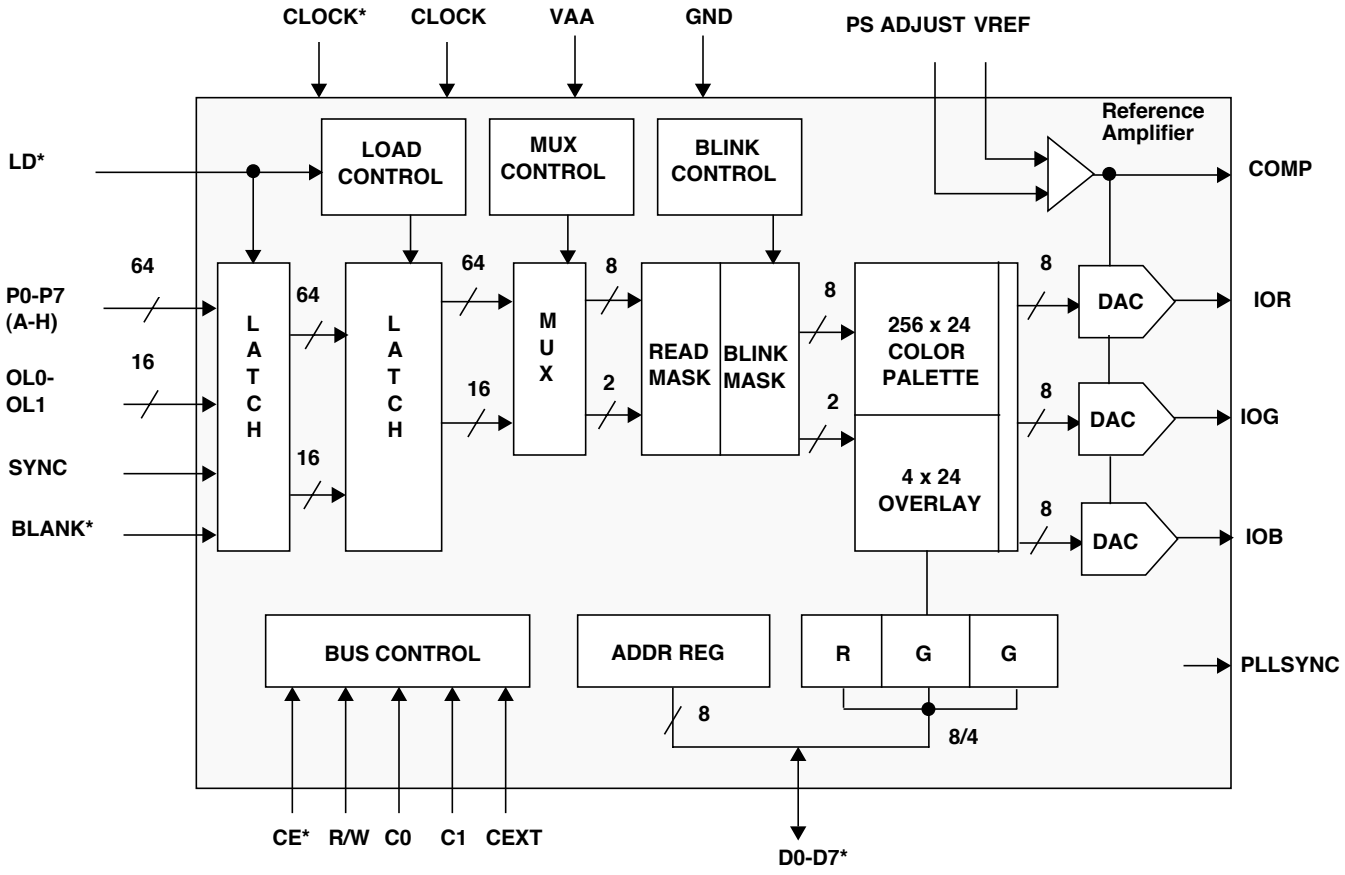


Figure 8-1 Bt467 Functional Block Diagram

8.1.1 MPU Interface

As shown in the functional block diagram, the Bt467 supports a standard MPU bus interface which allows the MPU direct access to the internal control registers and color/overlay palettes. The dual-port overlay registers allow color updating without contention with the display refresh process.

As shown in Table 8-1, the C0, C1, and CEXT control inputs, in conjunction with the internal address registers, specify which control register, color palette RAM entry, or overlay register will be accessed by the MPU. CEXT is used to specify Bt458 register compatibility or access to the extended register set.

The 8-bit address register (ADDR0–7) is used to address the internal RAM and registers, eliminating the requirement for external multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Table 8-1 Address Register (ADDR) Operations

ADDR0-7	CEXT	C1	C0	Addressed by MPU
$xx	X	0	0	Address Register
$00-$FF	X	0	1	Color Palette RAM
$00	X	1	1	Overlay Color 0
$01	X	1	1	Overlay Color 1
$02	X	1	1	Overlay Color 2
$03	X	1	1	Overlay Color 3
$00	X	1	0	ID Register ($80)
$01	X	1	0	Revision Register
$02	X	1	0	Reserved ($00)
$03	X	1	0	Reserved ($00)
$04	X	1	0	Read Mask Register
$05	X	1	0	Blink Mask Register
$06	X	1	0	Command Register 0
$07	X	1	0	Control/Test Register 1
$08	1	1	0	Command Register 1
$09	1	1	0	Command Register 2
$0A	1	1	0	Reserved ($00)
$0B	1	1	0	Test Register 2
$0C	1	1	0	Red Signature
$0D	1	1	0	Green Signature
$0E	1	1	0	Blue Signature
$0F	1	1	0	Reserved ($00)

8.1.2 Bt467 Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and

written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the read, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. In the Bt458 register compatibility mode, the MPU does not have access to these bits. However, in the extended register mode, the modulo three is accessible as read only register bits through command register 1. This provides information regarding the last color load before an interrupt was performed. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU.

Although the color palette RAM and overlay registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control register is also done through the address register in conjunction with the C0, C1 and CEXT inputs, as shown in Table 8-1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

Note, if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU. Figure 8-2 illustrates the MPU read/write timing of the Bt467.

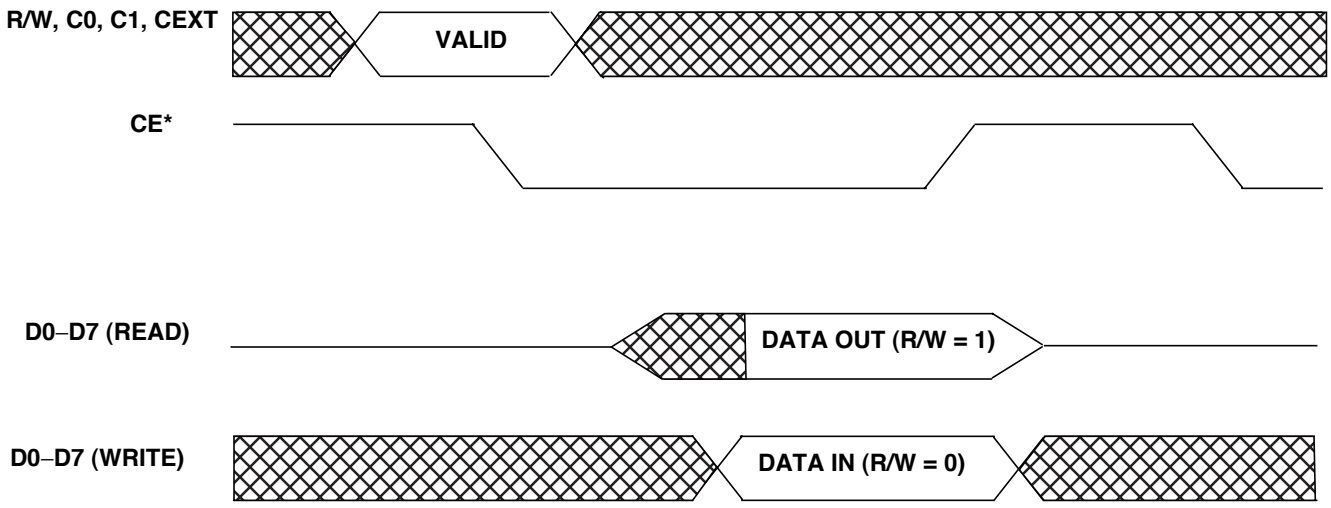


Figure 8-2 MPU Read/Write Timing

8.1.3 *Frame Buffer Interface*

To enable pixel data to be transferred from the frame buffer at TTL data rate, the Bt467 uses internal latches and multiplexers. As illustrated in Figure 8-3 below, on the rising edge of LD* and sync and blank, color and overlay for eight consecutive pixels are latched into the device. These inputs are (P0–P7 {A-H}) and the sync* blank inputs. With this configuration, the sync and blank timing will be recognized only with eight pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

Each clock cycle, the Bt467 outputs color information based on the {A} inputs, followed by the {B} inputs. etc., until all eight pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by the external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to the CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by eight, independent of the propagation delays of the LD* generation logic. As a result, the pixel and data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one clock cycle, but not more than eight clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

Only one rising edge of LD* should occur every eight clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*. Figure 8-3 shows the video input/output timing.

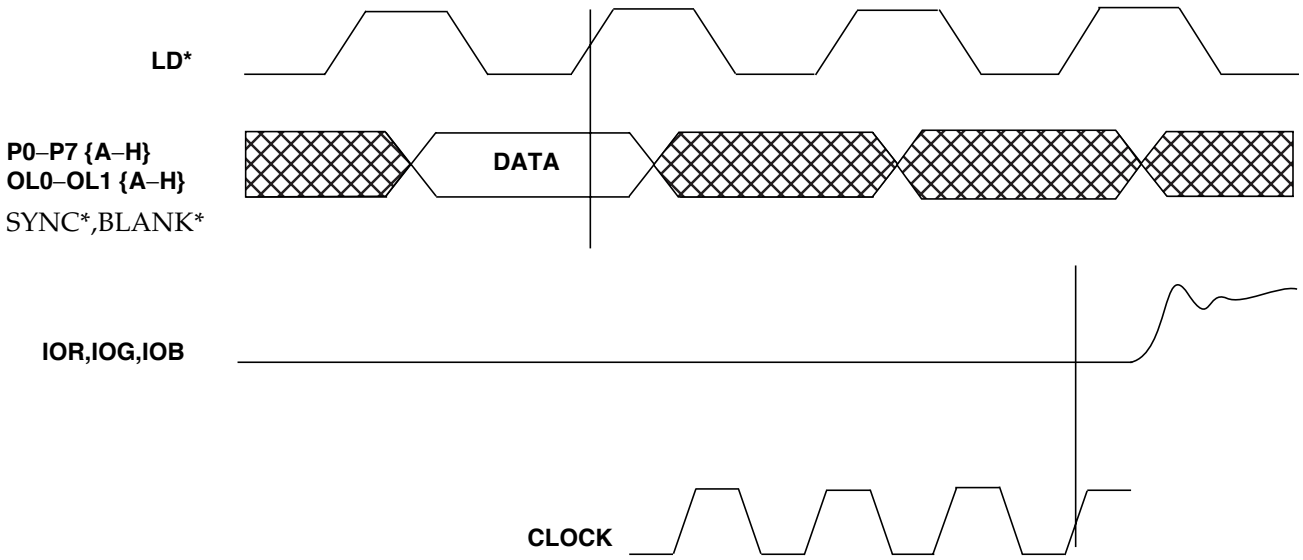


Figure 8-3 Video Input/Output Timing

8.1.4 Read and Blink Masking

Each clock cycle, 8 bits of color information (P0–P7) and 2 bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time, i.e., in the middle of the screen, the Bt467 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the least significant bit when addressing the color palette RAM. shows the truth table used for color selection.

Table 8-2 Palette and Overlay Select Truth Table

CR6	OL1	OL0	P7 - P0	Addressed by Frame Buffer
1	0	0	$00	Color palette entry $00
1	0	0**C**	$01	Color palette entry $01
:	:	:	:	:
1	0	0	$FF	Color palette entry $FF
0	0	0	$XX	Overlay color 0
X	0	1	$XX	Overlay color 1
X	1	0	$XX	Overlay color 2
X	1	1	$XX	Overlay color 3

8.1.5 Video Generation

Every clock cycle, the selected color information from the color palette RAMs or overlay registers is presented to the D/A converters.

The BLANK* input, pipelined to maintain synchronization with the pixel data, adds an appropriately weighted current to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 8-4 and Figure 8-5.

IOR, IOG, IOB	
MA	V
19.05	0.714
0.00	0.000

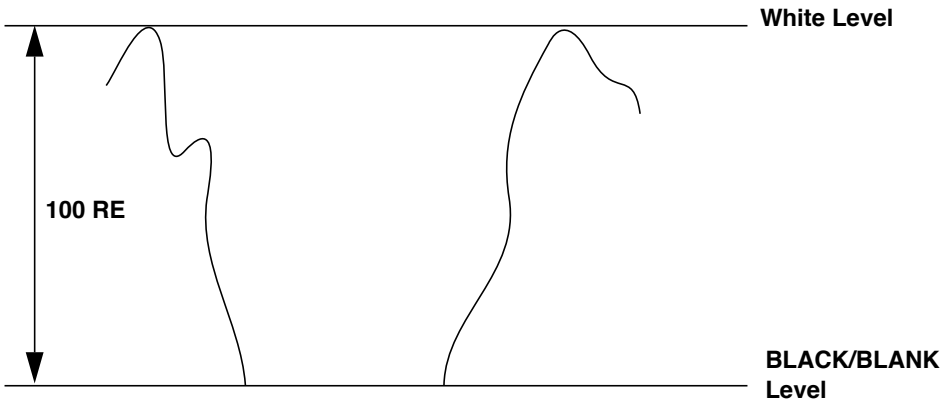


Figure 8-4 Composite Video Output Waveform (SETUP= 0 IRE)

Note – A 75-ohm doubly terminated load, RSET = 487 ohms, VREF = 1.235 V. Blank pedestal = 0 IRE. C2 = 0. RS-343A levels and tolerances assumed on all levels.

IOR, IOG, IOB	
MA	V
19.05	0.714
1.44	0.054
0.00	0.000

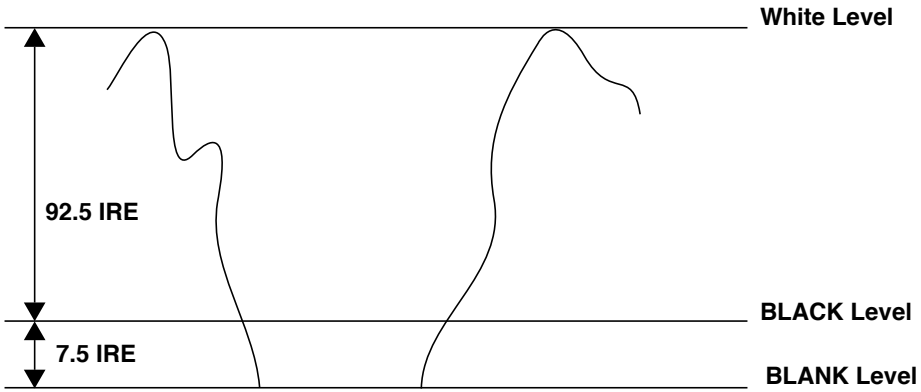


Figure 8-5 Composite Video Output Waveform (SETUP= 7.5 IRE)

Note – A 75-ohm doubly terminated load, RSET = 487 ohms, VREF = 1.235 V. Blank pedestal = 0 IRE. C2 =1. RS-343A levels and tolerances assumed on all levels.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. and Table 8-4 describe how the BLANK* input modifies the output levels.

Table 8-3 Video Output Truth Table (SETUP = 0 IRE)

Description	IOR, IOG, IOB (mA)	BLANK *	DAC Input Data
WHITE	19.05	1	$FF
DATA	Data	1	Data
BLACK	0	1	$00
BLANK	0	0	$xx

Note – Typical output with full-scale IOG = 19.05 mA. RSET = 487 ohms, VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 8-4 Video Output Truth Table (SETUP = 7.5 IRE)

Description	IOR, IOG, IOB (mA)	BLANK *	DAC Input Data
WHITE	19.05	1	$FF
DATA	Data + 1.44	1	Data
BLACK	1.44	1	$00
BLANK	0	0	$xx

Note – Typical output with full-scale IOG = 19.05 mA. RSET = 487 ohms, VREF = 1.235 V. Blank pedestal = 7.5 IRE.

The D/A converters on the Bt467 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current-steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full-scale output current against temperature and power supply variations.

8.1.6 CPU Interface

The CPU Interface allows the CPU to access the LUT and the internal registers of the RAMDAC. The type of access is determined by the Local Address lines 2 and 3 as follows:

LA3	LA2	Type of Access
0	0	Address Register (AR7–AR0)
0	1	Look-Up Table
1	0	Control Registers
1	1	Overlay Registers

Two internal counters allow fast access to the LUT and the Overlay Registers:

- An 8-bit address register (AR0–AR7) generates addresses for the Color Memory locations and the Control Registers. This register increments at the end of each third (blue) access when LA2 = 1. Thus the CPU does not have to rewrite the Address Register with consecutive values thereby saving CPU time and bus bandwidth for transfers to or from consecutive Color Memory locations. It operates as follows:

AR7–AR0	LA3	LA2	Location or Register Addresses
0x00-0xFF	0	1	Color LUT location 00 through FF
0x00	1	1	Overlay Register 0
0x01	1	1	Overlay Register 1
0x02	1	1	Overlay Register 2
0x03	1	1	Overlay Register 3
0x04	1	0	Read Mask Register
0x05	1	0	Blink Mask Register
0x06	1	0	Command Register
0x07	1	0	Test Register

AR7–AR0	LA12	LA3	LA2	Location or Register Addresses
$08	1	1	0	Command Register 1
$09	1	1	0	Command Register 2
$0A	1	1	0	Reserved ($00)
$0B	1	1	0	Test Register 2
$0C	1	1	0	Red Signature
$0D	1	1	0	Green Signature
$0E	1	1	0	Blue Signature
$0F	1	1	0	Reserved ($00)

- A modulo 3 Counter (ARa, ARb) controls which byte of the 24-bit Color Memory word is accessed. This register is not accessible by the CPU. It increments at the end of each CPU access with LA2 = 1 (color operations) and is reset to 0 at the end of each CPU access with LA2 = 0 (Control Registers operations). It operates as follows:

ARb	ARa	Color Byte Being Accessed
0	0	Red
0	1	Green

8.1.7 VRAM Interface

The RAMDAC accepts data from the VRAM at one eighth the rate that it presents RGB data to the monitor. This is done using the Input Buffer and the eight-to-one Input Multiplexer.

The rising edge of the LD* clock input loads the following signals into the Input Buffer:

- Pixel data inputs (PA<7..0> through PD<7..0>) from the VRAM
- The eight overlay data inputs (OL0<A..D> and OL1<A..D>) from the TEC block of the chip
- The BLANK* signal from the LSC chip, and the SYNC* signal, which is grounded

The pixel clock input (CLKN*/CLKP) gates each of the eight pixel bytes out of the Input Multiplexer in serial thus providing a eight-to-one multiplexing of the pixel bytes. The frequency of the pixel clock is eight times that of the load clock. The multiplexer first outputs the pixel from PA<7..0>, then PB through PH. It then repeats this cycle with the next bytes loaded from the VRAM.

Note that the 16 overlay data signals are also multiplexed eight-to-one. The multiplexer thus outputs OL0A and OL1A, then OLxB, OLxC, and OLxD.

Table 8-5 shows each of the possible read and write access modes.

Table 8-5 Truth Table for Bt467 Read and Write Operations

R/W	C1	C0	ADDR1	ADDR0	Function
0	0	0	x	x	Write Address Register; D0-D7 → ADDR2-9, 0 → ADDR0-1
0	0	1	0	0	Write Red Color; D0-D7 → RREG, increment ADDR0-9
0	0	1	0	1	Write Green Color; D0-D → GREG, increment ADDR0-9
0	0	1	1	0	Write Blue Color; D0-D → BREG, write color palette RAM, increment ADDR0-9
0	1	0	x	x	Write Control Register; D0-D7 → reg(ADDR), 0 → ADDR0-1
0	1	1	0	0	Write Red Color;D0-D → RREG, increment ADDR0-9
0	1	1	0	1	Write Green Color; D0-D → GREG, increment ADDR0-9
0	1	1	1	0	Write Blue Color; D0-D → BREG, write overlay register, increment ADDR0-9
1	0	0	x	x	Read Address Register; ADDR2-9 → D0-D7,0 → ADDR0-1
1	0	1	0	0	Read Color Palette Red; R0-R7 → D0-D7, increment ADDR0-9
1	0	1	0	1	Read Color Palette Green; G0-G7 → D0-D7, increment ADDR0-9
1	0	1	1	0	Read Color Palette Blue; B0-B7 → D0-D7, increment ADDR0-9
1	1	0	x	x	Read Control Register; reg(ADDR)→ D0-D7, 0 → ADDR0-1
1	1	1	0	0	Read Overlay Palette Red; R0-R7→ D0-D7, increment ADDR0-9
1	1	1	0	1	Read Overlay Palette Green;G0-G7→ D0-D7, increment ADDR0-9
1	1	1	1	0	Read Overlay Palette Blue;B0-B7→ D0-D7, increment ADDR0-9

Key:

→ = gets the value of

RREG = Red Byte Register

GREG = Green Byte Register

BREG = Blue Byte Register

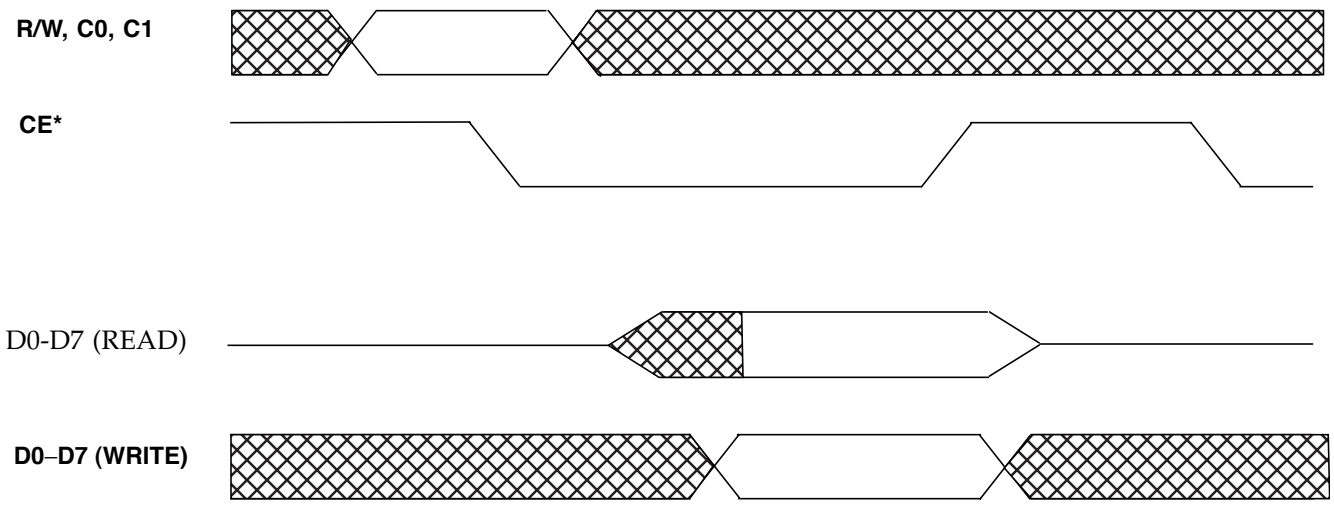


Figure 8-6 Host MPU Read/Write Timing

8.1.8 *Internal Multiplexing*

The LD* may be phase shifted, in any amount, relative to CLOCK to simplify the frame buffer interface timing. It enables the LD* signal to be derived externally dividing the CLOCK by eight. This should be independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of CLOCK phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD signal by at least one, but not more than eight clock cycles. This load signal transfers the latched pixel and overlay data into a second set of latches which are then internally multiplexed at the CLOCK rate (up to 227 MHz).

Since 8:1 multiplexing is specified, only one rising edge of LD* should occur every eight CLOCK cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal and will continuously attempt to resynchronize itself to LD*.

8.1.9 Color Selection

The eight pixel data bits and two overlay bits gated out of the multiplexer during each pixel clock cycle are processed by the Blink and Read Mask, and by the Command Register. This information is then used to select an entry in the Color LUT or an Overlay Register to provide color information.

The 8-bit Read Mask Register selectively enables or disables bit planes from being presented to the Color LUT. The 8-bit Blink Mask Register selectively enables or disables blinking on a bit plane. Bit 4 and 5 of the Command Register determine the blink-rate duty cycle. The counter that generates the internal blink clock is incremented during the vertical retrace intervals. These intervals are detected when BLANK* is low for a period of at least 256 load clock cycles.

On the rising edge of the CLOCK cycle, eight bits of color information (P0– P7) and two bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

Note, P0 is the LSB when addressing the color palette RAM. Table 8-6 shows the truth table used for color selection.

Table 8-6 Palette and Overlay Select Truth Table

CR6	OL1	OL0	P7 - P0	Addressed by Frame Buffer
1	0	0	$00	Color palette entry $00
1	0	0	$01	Color palette entry $01
:	:	:	:	:
1	0	0	$FF	Color palette entry $FF
0	0	0	$XX	Overlay color 0
X	0	1	$XX	Overlay color 1
X	1	0	$XX	Overlay color 2
X	1	1	$XX	Overlay color 3

8.1.10 Overlay Color Selection

The four 24-bit Overlay Registers provide four different overlay colors that are selected by the two overlay bits. Bits 0 and 1 of the Command Register act as a read mask, and bits 2 and 3 act as a blink mask on the overlay inputs. Thus an overlay output (OVLADDR0 or OVLADDR1) is present only when the corresponding read mask bit and blink mask bit are true. When the blink mask is enabled, an internal blink clock turns the overlay output off and then on.

The Overlay Register is selected as shown below. Note that when OVLADDR1 = 0 and OVLADDR0 = 0, bit 6 of the Command Register selects between Overlay Register 0 and the Look-Up Table output addressed by the eight pixel bits.

OVLADDR1	**VLADDR0**	**Bit 6 = 0**
0	0	Overlay Register 0
0	1	Overlay Register 1
1	0	Overlay Register 2
1	1	Overlay Register 3

8.1.11 Overlay Select Input Lines

The OL0-OL1 {A-H} overlay select inputs (TTL compatible) are latched on the rising edge of LD*. They, in conjunction with bit 6 of the command register, specify which palette is to be used for color information. See table below.

Table 8-7 Signals Between RAMDAC Chip and the TEC Block

OL1	**OL0**	**CR6 = 1**
0	0	Color Pallette RAM
0	1	Overlay Color 1
1	0	Overlay Color 2
1	1	Overlay Color 3

8.1.12 User Accessible Registers

The user can access the following registers: Address, Command, Read Mask, Blink Mask, and Test.

8.1.13 Address Register

The Address Register is accessed when LA3 and LA2 are 0. If LWRITE* is low, local data bus lines LD<31..24> are loaded into the Address Register. If LWRITE* is high, the contents of the Address Register are loaded onto local data bus lines LD<31..24>.

8.1.14 Command Register

The Command Register is an 8-bit register located at address 0x06. Table 8-8 describes the operation of this register.

Table 8-8 Command Register Definition

Bit	Name	Definition	Description
CR7	Multiplex Select	0 = 8:1 Multiplexing 1 = 8:1 Multiplexing	Specifies 8:1 multiplexing for pixel and overlay data. It is possible to reset the pipeline delay of the Bt467 to a fixed number of clock cycles. Set to 0.
CR6	RAM Enable	0 = Use Overlay Color 0 1 = Use Color Palette RAM	When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information. Set to 1.
CR5, CR4	Blink Rate Selection	00 = 1.024 Seconds (75/25) 01= 0.512 Seconds (50/50) 10= 1.024 Seconds (50/50) 11 = 2.048 Seconds (50/50)	Specify the blink rate cycle time and duty cycle of the internal blink clock assuming a 60 Hz noninterlaced or 30 z interlaced refresh rate. For applications having other refresh rates, i.e., 57 Hz noninterlaced, the blink rate is determined by scaling the specified values (i.e., multiplying by 57/60). The numbers in parentheses specify the duty cycle (% on/off). Set to 00.
CR3	OL1 Blink Enable	0 = Disable Blinking 1 = Enable Blinking	When set to 1, this bit forces the OL1 {A-H} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL1 {A-H} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one. Set to 0.

Table 8-8 Command Register Definition

Bit	Name	Definition	Description
CR2	OL0 Blink Enable	0 = Disable Blinking 1 = Enable Blinking	When set to 1, this bit forces the OL0 {A-H} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL0 {A-H} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one. Set to 0.
CR1	OL1 Display Enable	0 = Disable 1 = Enable	When set to 0, this bit forces the OL1{A-H} inputs to a logical 0 before selecting the palettes. When set to 1, it does not affect the value of the OL1 {A-H} inputs. Set to 1.
CR0	OL0 Display Enable	0 = Disable 1 = Enable	When set to 0, this bit forces the OL0{A-H} inputs to a logical 0 before selecting the palettes. When set to 1, it does not affect the value of the OL0 {A-H} inputs. Set to 1.

8.1.15 Command Register 1

The Command Register 1 may be written to or read by the MPU at any time, and is not initialized. CR1 corresponds to data bus bit D0. The following Table describes the Command Register bits.

Table 8-9 Command Register 1 Definition

Bit	Function	Description
CR17, CR16	Address counters: (0,0) Red (0,1) Green (1,0) Blue (1,1) Undefined	This is a read only register bit which specifies the location of the a or b address of the module. This is useful in determining the last location written. These bits are read only.
CR15	Reserved (logical zero)	
CR14	Reserved (logical zero)	
CR13	Reserved (logical zero)	
CR12	Reserved (logical zero)	
CR11	Reserved (logical zero)	
CR10	Reserved (logical zero)	

8.1.16 Command Register 2

The Command Register 2 may be written to or read by the MPU at any time, and is not initialized. CR20 corresponds to data bus bit D0. Table 8-10 describes the Command Register bits.

Table 8-10 Command Register 2 Definition

Bit	Function	Description
CR27	Reserved (logical zero)	
CR**26**	Pedestal Enable (0) 0 IRE Pedestal (1) 7.5 IRE Pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load Palette RAM Select (00) Normal (01) Red RAMDAC (10) Green RAMDAC (11) Blue RAMDAC	If (00) is specified, color data is loaded into the Bt467 using three write cycles (red, green, and blue) and color data is output using three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt467 to emulate a single-channel RAMDAC using only the green channel. The Bt467 expects color data to be input and output using (red, blue, and green) cycles. The exact value indicates during which one of the three color cycles it is to load or output color information. The value is loaded into or read from the green palette RAM.
CR23	PLL Generate (0) SYNC (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* for generating PLL information.
CR22	PLL/SYNC	This bit specifies whether the PLL/SYNC information is to be output.
CR21	PLL/SYNC Select (0) PLL (1) SYNC	This bit specifies whether the PLL/SYNC output uses PLL or SYNC.
CR20	Test Mode Select (0) Signature Analysis Set (1) Data strobe Test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test results for both test methods.

8.1.17 Read Mask Register

The Read Mask Register is an 8-bit register located at address 0x04. It is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A–H}) and D7 corresponds to bit plane 7 (P7 {A–H}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized.

Bit 0 masks inputs PA<0> through PH<0>, bit 1 masks inputs PA<1> through PH<1>, and so on. Overlay plane masking is controlled by bits 1 and 0 of the Command Resister.

8.1.18 Blink Mask Register

The Blink Mask Register is an 8-bit register located at address 0x05. It is used to enable (logical one) or disable (logical 0) a bit plane from blinking at the blink rate and duty cycle specified by the command register. When enabled, the bit plane toggles between its original value and logical 0 at the selected rate and duty cycle. D0 corresponds to bit plane 7 (P7 {A–H}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized. Overlay plane masking is controlled by bits 3 and 2 of the Command Resister.

8.1.19 ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different from each RAMDAC. For the Bt467, the value read by the MPU is $80. Data written to this register is ignored.

8.1.20 Revision Register

This 8-bit register is a read only register, specifying the revision of the Bt467. The four most significant bits specify the revision letter in hexadecimal form. The four least significant bits do not represent any value and should be ignored.

8.1.21 Test Register 1

The Test Register is an 8-bit register located at address 0x07. It can read back data presented to the DACs from the Color Memory (either pixel or overlay data). The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time and is not initialized. When writing to the register, the upper 4 bits (D4–D7) are ignored. Bits 7 through 4 contain color information and bits 3 through 0 contain control information. Table 8-11 defines the register contents.

Table 8-11 Test Register 1 Contents

D7-D4	Color Information (4 bits of Red, green, or Blue)
D3	Low (logical one) or high (logical zero) nibble
D2	Blue Enable
D1	Green Enable
D0	Red Enable

To use the test register, the host MPU writes to it, setting one, and only one, of the red, green, and blue bits. These bits specify which four bits of color information the MPU wishes to read (R0–R3, G0–G3, B0–B3, R4–R7, G4–G7, or B4-B7). When the MPU reads the test register, the four bits of color information from the DAC inputs are contained on the upper four bits, and the lower four bits contain the red, green, blue, low, or high nibble enable information that was written previously.

Note – Either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

To read the upper four bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the read enable bit. The MPU then proceeds to read the test register, keeping the pixel data stable. This results in D4-D7 containing R4-R7 color bits, and D0-D3 containing (red, green, blue, low, or high nibble) enable information is shown below.

Table 8-12 Reading the Test Register 1

MPU - Bit	Color
D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

8.1.21.1 Red, Green, and Blue Output Signature Registers

Signature Operation

These three 8-bit signature registers may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the output signature registers while BLANK* is a logical zero to load the seed value. The output signature registers use data being loaded into the output DACs to calculate the signatures.

By loading a test display into the frame buffer, a given value for the red, green, and blue signature registers will be returned if all circuitry is working properly.

Data Strobe Operation

If command bit CR20 selects “data strobe testing”, the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–H) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–H) is to be captured.

Table 8-13 Test Register 2

D2-D0	Selection
000	Pixel A
001	Pixel B
010	Pixel C
011	Pixel D
100	Pixel E
101	Pixel F
110	Pixel G
111	Pixel H

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional.

D7	D6	D5	D4	D3
Red Select	Green Select	Blue Select	145 mV Ref.	Result Select

Table 8-14 lists the valid comparison combinations. A logical one enables that function to be compared. The result is D3. The output levels of the DACs should be constant for 5 µSec to allow enough time for detection. The capture occurs over one LD* period set by a logic one at any time of the pixel pin (value = A-H).

For normal operations, D3–D7 must be a logical zero.

Table 8-14 Valid Comparison Combinations

D7-D4	Description	If D3=1	If D3 =0
0000	Normal operation	-	-
1010	Red DAC compared to blue DAC	Red>Blue	Blue>Red
1001	Red DAC compared to 145 mV reference	Red>145 mV	Red<145 mV
0110	Green DAC compared to blue DAC	Green>145 mV	Blue>Green
0101	Green DAC compared to 145 mV reference	Green>145 mV	Green<145 mV

8.1.22 Test Register 2

This 8-bit register is used for testing the Bt467. Signature analysis is done on every eighth pixel. D0–D2 are used for 8:1 multiplexing to specify whether to use the A, B, C, D, E, F, G, or H pixel inputs as shown in Table 8-13.

8.1.23 Signal Descriptions

The input and output signals of the RAMDAC chip are described in Table 8-15 and Table 8-16. Table 8-17 shows the pin list for the Bt467. Note that the I/O column indicates the signal input or output direction from the RAMDAC chip's point of views. Also note that the signal names in these tables are the names used on the TGX schematic diagram.

Table 8-15 Signals Between RAMDAC Chip and the LSC Chip

Name	Pin	I/O	Description
BLANK*	TBD	I	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored. It overrides the color pixel and overlay data to force the RED, GREEN, and BLUE video output signals to their blanking levels. Blanking is required during the monitor's vertical and horizontal retrace period.
CS_DAC*		I	Chip Select signal that enables the CPU Interface logic. Data on the Local Data bus LD<31.. 24> is internally latched on the rising edge of CS_DAC* during write operations.
LD*		I	Load control input (TTL compatible). The P0-P7 {A-E}, OL0-OL1 {A-E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. This signal is one-fourth the rate of the pixel clock frequency.

Table 8-16 Bt467 Pin Descriptions

Pin Name	Pin Numb	I/O	Description
BLANK*	TBD	I	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*		I	Composite sync control input (TTL compatible). A logical zero on this input switches off a current source on the IOG output. SYNC* does not override any other control or data input. It should be asserted only during the blanking interval. It is latched on the rising edge of LDCK*.
LD*		I	Load control input (TTL compatible). The P0-P7 {A-H}, OL0-OL1 {A-H}, BLANK*, and SYNC* inputs are latched on the rising edge of the LD*. This signal is one-fourth the rate of the pixel clock frequency. LD*, while it is either 1/4 or 1/5 the CLOCK rate, may be phase independent of the CLOCK and CLOCK* inputs.
P0-P7 ({A-H)		I	Overlay select input (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. Either four or five consecutive pixels (up to eight bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused pixel inputs must be connected to the regular PCB ground plane. Note, that the {A} pixel is output first, followed by the {B} pixel, etc., until all four or five pixels have been output. Then the cycle repeats.
Ol0-OL1 {A-H)			Overlay select input (TTL compatible). These control inputs are latched on the rising edge of LD*, and in conjunction with bit 6 of the command register, specify which palette is to be used for color information as shown below:

OL1	OL0	CR6 = 1	CR6 = 0
0	0	Color Pallette RAM	Overlay Color 0
0	1	Overlay Color 1	Overlay color 1
1	0	Overlay Color 2	Overlay color 2
1	1	Overlay Color 3	Overlay color 3

When accessing the overlay palette, the P0-P7 {A-H} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for eight consecutive pixels are input through this port. Unused inputs should be connected to GND.

R, G, B	TBD	O	Red, green, and blue video current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-ohm coaxial cable.

Table 8-16 Bt467 Pin Descriptions

Pin Name	Pin Numb	I/O	Description
PLL/SYNC	See Table 8-16		Phase lock loop current input. This high-impedance current source is used to enable multiple Bt467s to be synchronized with sub-pixel resolution when used with an external PLL. This function is accessible through the extended command register. A logical one on the BLANK* input results in no current being output onto this pin, while a logical zero results in the following current being output. PLL (mA) = 3,227 * VREF (V)/RSET (ohms) If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 ohms).
AGND (GND)			Analog ground. All GND pins must be connected
VAA		PG	Analog power. All VAA pins must be connected.
COMP		PG	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 *u*F ceramic capacitor must be connected between this pin and VAA.
FS ADJUST		I	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal. Using the oscilloscope, the voltage at this pin should be approximately equal to the voltage at the VREF pin. The relationship between RSET and the full scale output current on IOG is: RSET (ohms) = 10,684* VREF (V)/IOG (mA) The full scale output current on IOR and IOB for a given RSET is: IOR, IOG, IOB, (mA) = 7,457 * VREF (V) / RSET (ohms)
VREF	TBD	I	Voltage reference input. An external reference circuit must supply this input with a 1.235V (typical) reference. A 0.01 *u*F ceramic capacitor must be used to decouple this input to VAA. The use of a resistor network to generate the reference is not recommended as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs.
CLK, CLK_L*		I	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5V) operation. The clock rate is typically the pixel clock rate of the system.

Table 8-16 Bt467 Pin Descriptions

Pin Name	Pin Numb	I/O	Description
CE*	See Table 8-16	I	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operation, data is internally latched on the rising edge of the CE*.
R/W		I	Read/Write control input. To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, the CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1, CEXT		I	Command control inputs (TTL compatible). C0, C1, and CEXT specify the type of read or write operation being performed. They are latched on the falling edge of CE*.
D0-D7			Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D0 is the least significant bit.

Table 8-17 Bt 467 Pin List

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	K1	P5A	K15	D0	B9
SYNC*	J2	P5B	J15	D1	B8
LD*	K3	P5C	K13	D2	A10
CLOCK	J1	P5D	K14	D3	A9
CLOCK*	K2	P5E	L14	D4	C10
		P5F	L15	D5	B10
P0A	P1	P5G	M15	D6	B11
P0B	P2	P5H	L13	D7	A11
P0C	N2				
P0D	N1	P6A	D15	VAA	C3
P0E	M1	P6B	E15	VAA	C7
P0F	L3	P6C	F15	VAA	C8
P0G	L2	P6D	F14	VAA	C13
P0H	M2	P6E	G14	VAA	D4
		P6F	G15	VAA	G13
P1A	R4	P6G	J14	VAA	H3
P1B	N5	P6H	H15	VAA	H13
P1C	N4			VAA	J3

Table 8-17 Bt 467 Pin List

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
P1D	P4	P7A	B15	VAA	N3
P1E	R2	P7B	B14	VAA	N13
P1F	R3	P7C	C14		
P1G	P3	P7D	C15	GND	A5
P1H	R1	P7E	E14	GND	A7
		P7F	E13	GND	C4
P2A	P7	P7G	F13	GND	C9
P2B	R7	P7H	D14	GND	D13
P2C	R6			GND	G3
P2D	N7	OL0A	D1	GND	H2
P2E	N6	OL0B	E3	GND	H14
P2G	P5	OL0D	D2	GND	M3
P2H	R5	OL0E	B1	GND	N12
		OL0F	C1		
P3A	R10	OL0G	C2	GND	A2
P3B	P10	OL0H	A1	reserved	L1
P3C	P9			reserved	A12
P3D	N9	OL1A	G2	reserved	C12
P3E	R8	OL1B	H1	reserved	A14
P3F	R9	OL1C	F1	reserved	B13
P3G	N8	OL1D	G1	reserved	C11
P3H	P8	OL1E	F3	reserved	B12
P4A	M13	OL1H	E1	reserved	A15
P4B	M14	OL1H	E1	reserved	P13
P4C	P15			reserved	R12
P4D	N15	IOR	A8	reserved	P11
P4E	N14	IOG	B7	reserved	N10
P4F	R15	IOB	A6	reserved	R13
P4G	R14	PLL/SYNC*	A4	reserved	P12
P4H	P14			reserved	N11
		CE*	B2	reserved	R11

Table 8-17 Bt 467 Pin List

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
COMP	C6	R/W	B3		
FS ADJUST	A3	C0	B5		
VREF	B6	C1	C5		
		CEXT	B4		

Single Chip GX Cards Configuration

This chapter describes different GX cards configurations. It contains specific information about a particular GX card that is not covered in the previous chapters. We recommend that you read the first three chapters of this manual which contain generic information which applies to all single chip GX cards.

Each subsection in this chapter covers the following topics:

- Hardware platform
- Specifications
- Block diagram
- Memory devices
- Timing diagrams

9.1 Single Chip GX Possible Configurations

The single chip GX can be initialized to 12 card configurations. Four of them are not available (N/A) due to two reasons: 1) VRAM bus width is only 32 bits (the Single Chip GX requires a 64-bit bus); 2) four sets of control lines are required (the Single Chip GX has only two).

Note – There are four single chip GX card products at this time: GX, GXplus, TurboGXplus, and TurboGX (still unreleased). In addition, SPARCstation Sunergy and SPARCstation IPX have the GX chip on the CPU board. Table 9-1 (provided for informational purposes only), describes all the addressing modes to which the single chip GX can be initialized.

Table 9-1 Single Chip GX Possible Configurations

Total VRAM Memory	Memory Device Type	DAC* MUX	Single Buffer Support	Double Buffer Support	High Res	Product Name	Code Name
1 MB	128K X 8	4	Yes	No	No	GX/IPX	LegoSC Jr.
1 MB	128K X 8	8	Yes	No	No	LX	LegoSC Sr.
1 MB	256K X 4	4	-	-	-	N/A	
1 MB	256K X 4	8	-	-	-	N/A	
1 MB	128K X 8	4	Yes	No	No	TurboGX	Quadro Sr.
2 MB	128K X 8	4	Yes	Yes	No	TBD	Duplo Jr.
2 MB	128K X 8	8	Yes	Yes	Yes	LX with VSIMM	Duplo Sr.
2 MB	256K X 4/ 256K X 8	4	Yes	No/Yes **	No	TBD	LegoHR Jr.
2MB	256K X 4/ 256K X 8	8	Yes	No/Yes **	No	TBD	LegoHR Sr.
4 MB	128K X 8	4	-	-	-	N/A	
4 MB	128K X 8	8	-	-	-	N/A	
4 MB	256K X 4/ 256K X 8	4	Yes	Yes	No	GXplus	Quadro Jr.
4 MB	256K X 4/ 256K X 8	8	Yes	Yes	Yes	TurboGX plus	Quadro Sr.

Legend:

N/A = Not Available

TBD = To Be Defined

* = DAC MUX Size: 4 implies Bt458 compatible RAMDAC; 8 implies Bt467 compatible RAMDAC

** = TurboGX

9.2 GX Card

The GX card is an SBus compatible 8-bit color/greyscale graphics accelerator card. It is 100% software backward compatible with the LegoS4 and LegoP4. It can be used either with the old 66 MHz Sun color monitor or the new 76 MHz Sun color monitor. The GX card is a single-wide (146.7 mm long by 83.82 mm wide) SBus expansion card that conforms to the Sun single-wide Sbus card specification. Refer to Chapter 1 for additional information.

Figure 9-1 shows the GX card layout.

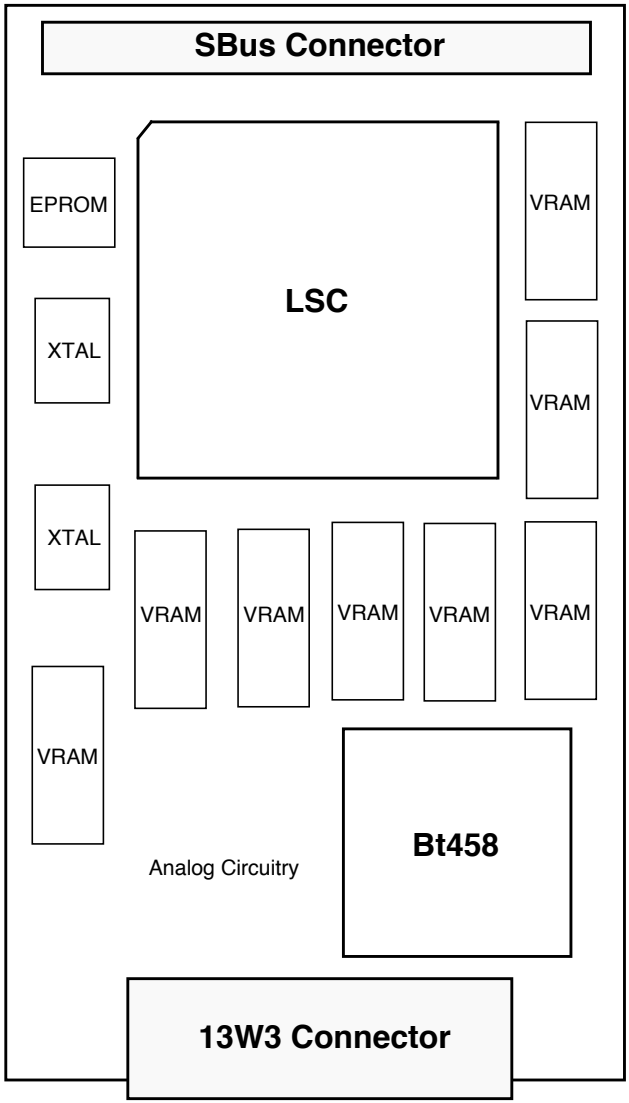


Figure 9-1 GX Card Layout

9.2.1 Hardware Platform

The GX card is supported on various SBus based SPARCstations and SPARCsystems. The GX chip is present on the SPARCstation IPX and SPARCstation Sunergy systems. Here is a list of SPARCstations and SPARCsystem machines on which the GX card is supported:

- SPARCstation 1
- SPARCstation 1+
- SPARCstation IPC
- SPARCstation 2
- SPARCstation IPX
- SPARCstation 10
- SPARCstation Sunergy (unreleased product)
- SPARCsystem 630 MP
- SPARCsystem 670 MP
- SPARCsystem 690 MP

Refer to the *GX Installation Guide* (800-5111) for GX configuration options.

9.3 GX Card Specifications Summary

Length: 146.70 mm

Width: 83.82 mm

Weight: 5.7 Oz.

9.3.1 Electrical Specifications

9.3.1.1 Input Requirements

Current: 1 amp (typical), 1.5 amps (worst case)

Power Requirements: +5 volts ±5%

Heat dissipation: 5 watts (approximate)

Load Condition: Running special code designed for exercising the frame buffer to the maximum power (not typical of normal applications)

9.3.2 GX Environmental and Reliability Specifications

Table 9-2 Environmental and Reliability Specifications, GX Card

Reliability Parameters	Specification
Temperature, operating	0 and 40 degrees C
Temperature, storage	-20 and 80 degrees C
Relative humidity	5% to 80% (non-condensing)
Altitude, operating	0 to 10,000 feet (0 to 3048 meters
Altitude, storage	0 to 40,000 feet (0 to 9144 meters)
MTTR	30 minutes
MTBF	163,000 hours

9.3.3 Performance

Assuming 23 MHz (92.9405 MHz/4) clock and 1152x900 resolution:

Horizontal fill: 120 Mpixels per second

Vertical fill: 4.8 Mpixels per second

Vector and Polygon Performance: Depends on the CPU platform and software efficiency

9.3.4 Double Buffer Support

Color map double buffering allows two 4-bit buffers. No hardware double buffering is supported.

9.3.5 DAC

Bt458 compatible

9.3.6 Resolutions

1152 x 900 @66 Hz

1152 x 900 @76 Hz

1024 x 800 @84 Hz

9.3.7 Interface Requirements

Connector type: SBus

9.3.8 Agency Certification

FCC Class B

DOC Class B

VCCI Class 2

UL

CSA

TUV

9.3.9 Compatibility

SBus compatible

9.3.10 Memory Devices

Uses eight 128k x 8 100 nS VRAMs. Refer to Chapter 5 for additional information.

9.3.11 Component Packaging

The LSC is a 223-pin package in a 18 x 18 grid of pins numbered linearly from 1 through 324. Actually there is no pin 1 on the chip or on the socket. It is intentionally omitted to eliminate any possibility of misalignment. Pin 2 is the leftmost pin in the corner on the top row (near the SBus connector) on the component side.

Two alphanumeric pin identification schemes have been used on the card. In addition to pin numbers, pins can be identified with their relationship to the alphanumeric rows 1 to 18 and A to V. If you already know the signal name and want to know the alpha or numeric pin name, refer to Table 4-8.

9.3.12 Video Timing Diagrams

Refer to Chapter 5 for details.

9.3.13 Video Memory Architecture

The following figures show video memory data side and video side architecture for the GX card.

Figure 9-2 shows the GX card video memory data side architecture.

Figure 9-6 shows the GX card video memory video side architecture.

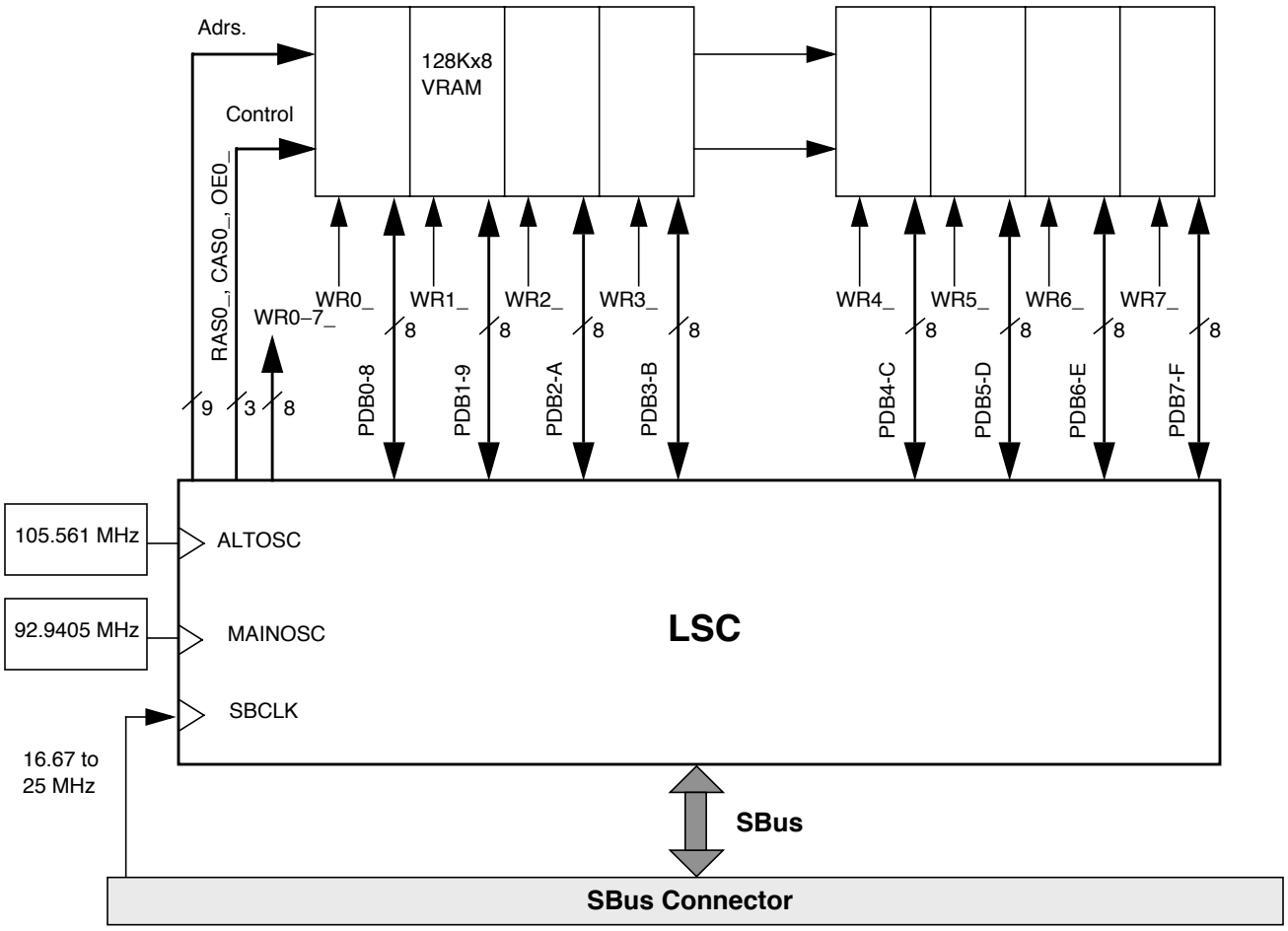


Figure 9-2 GX card Video Memory Data Side Architecture

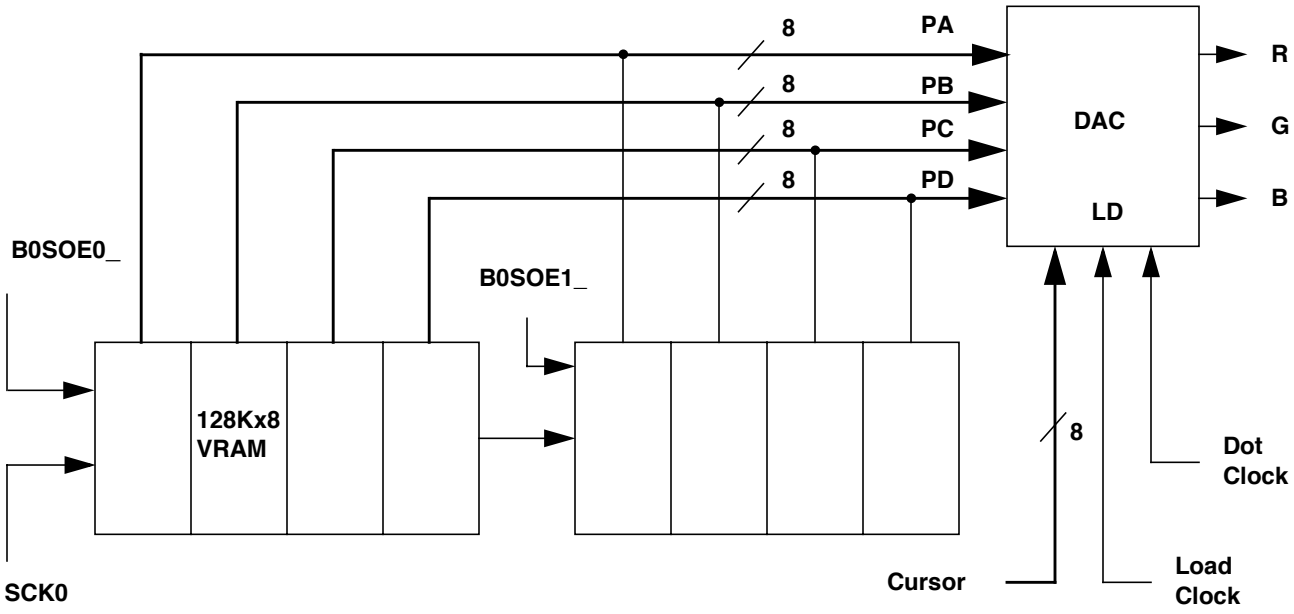


Figure 9-3 GX Card Video Memory Video Side Architecture

9.4 GXplus Card

The GXplus card is an SBus compatible 8-bit color/greyscale graphics accelerator card. It is 100% software backward compatible with the LegoS4 and LegoP4. It can be used either with the old 66 MHz Sun color monitor or the new 76 MHz Sun color monitor. The GXplus is a double-wide (146.7 mm long by 170.28 mm wide) SBus expansion card which conforms to Sun double-width Sbus card specification. Refer to Chapter 1 for additional information.

Figure 9-4 shows the GXplus card layout.

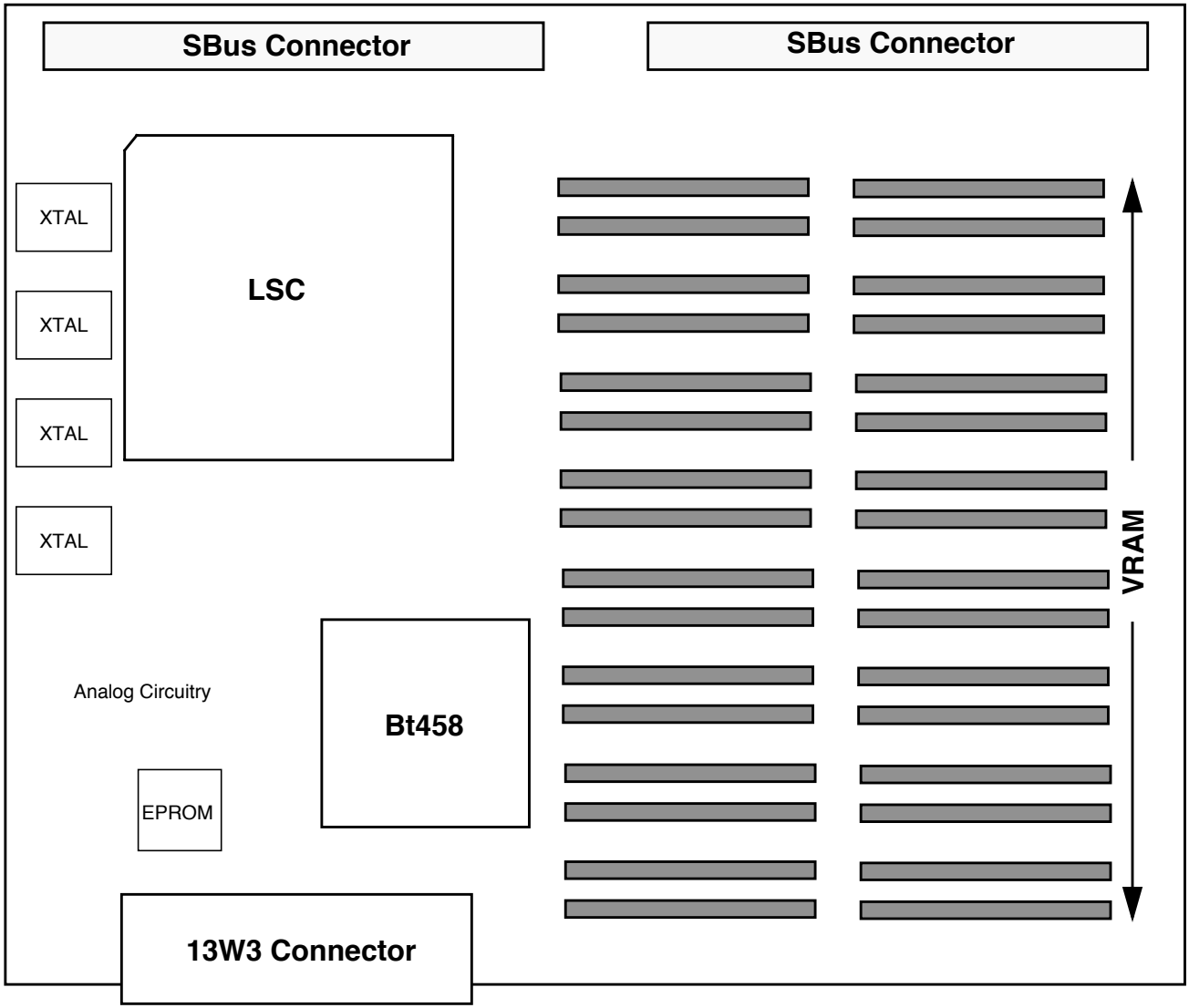


Figure 9-4 GXplus Card Layout

9.4.1 Hardware Platform

The GXplus card is currently supported on the following SPARCstations and SPARCsystem machines:

- SPARCstation 2
- SPARCstation IPX
- SPARCstation 10
- SPARCsystem 630 MP
- SPARCsystem 670 MP
- SPARCsystem 690 MP

9.5 GXplus Specifications Summary

9.5.1 Physical Specifications

Length: 146.70 mm

Width: 170.28 mm

Weight: 11.0 Oz.

9.5.2 Electrical Specifications

9.5.2.1 Input Requirements

Current: 2.5 amps

Power Requirements: +5 volts ±5%

Heat dissipation: 12.5 watts

Load Condition: Running special code designed for exercising the frame buffer to the maximum power

Load Condition: Running special code designed for exercising the frame buffer to the maximum power

9.5.3 GXplus Environmental and Reliability Specifications

Table 9-3 GXplus Card Environmental and Reliability Specifications

Reliability Parameters	Specification
Temperature, operating	0 to 40 degrees C
Temperature, storage	-20 to 80 degrees C
Relative humidity	5% to 80% (non-condensing)
Altitude, operating	0 to 10,000 feet (0 to 3048 meters
Altitude, storage	0 to 40,000 feet (0 to 9144 meters)
MTTR	30 minutes
MTBF	135,000 hours

9.5.4 Performance

Assuming 23 MHz (92.9405 MHz/4) clock and 1152 x 900 resolution.

Horizontal fill: 120 Mpixels per second

Vertical fill: 4.8 Mpixels per second

Vector and Polygon Performance: Depends on the CPU platform and software efficiency

9.5.5 Double Buffer Support

Double buffering allows two 8-bit buffers.

9.5.6 DAC

Bt458 compatible

9.6 Resolutions

1152x900 @66 Hz

1152x900 @76 Hz

1024x800 @84 Hz

1280x1024 @67 Hz

9.7 Interface Requirements

Connector type: SBus

9.8 Agency Certification

FCC Class B

DOC Class B

VCCI Class 2

UL

CSA

TUV

9.9 Compatibility

SBus compatible

9.9.1 Memory Devices

Uses thirty two 256k x 4 100 nS VRAMs. Refer to Chapter 5 for additional information.

9.9.2 Component Packaging

Refer to the GX card specifications described earlier. The GXplus uses the same chip.

9.9.3 Video Timing Diagrams

Refer to Chapter 5 for details.

9.9.4 Video Memory Architecture

The following figures show the video memory data side and video side architecture for the GXplus.

Figure 9-5 shows the GXplus video memory data side architecture.

Figure 9-6 shows the video memory video side data architecture for the GXplus.

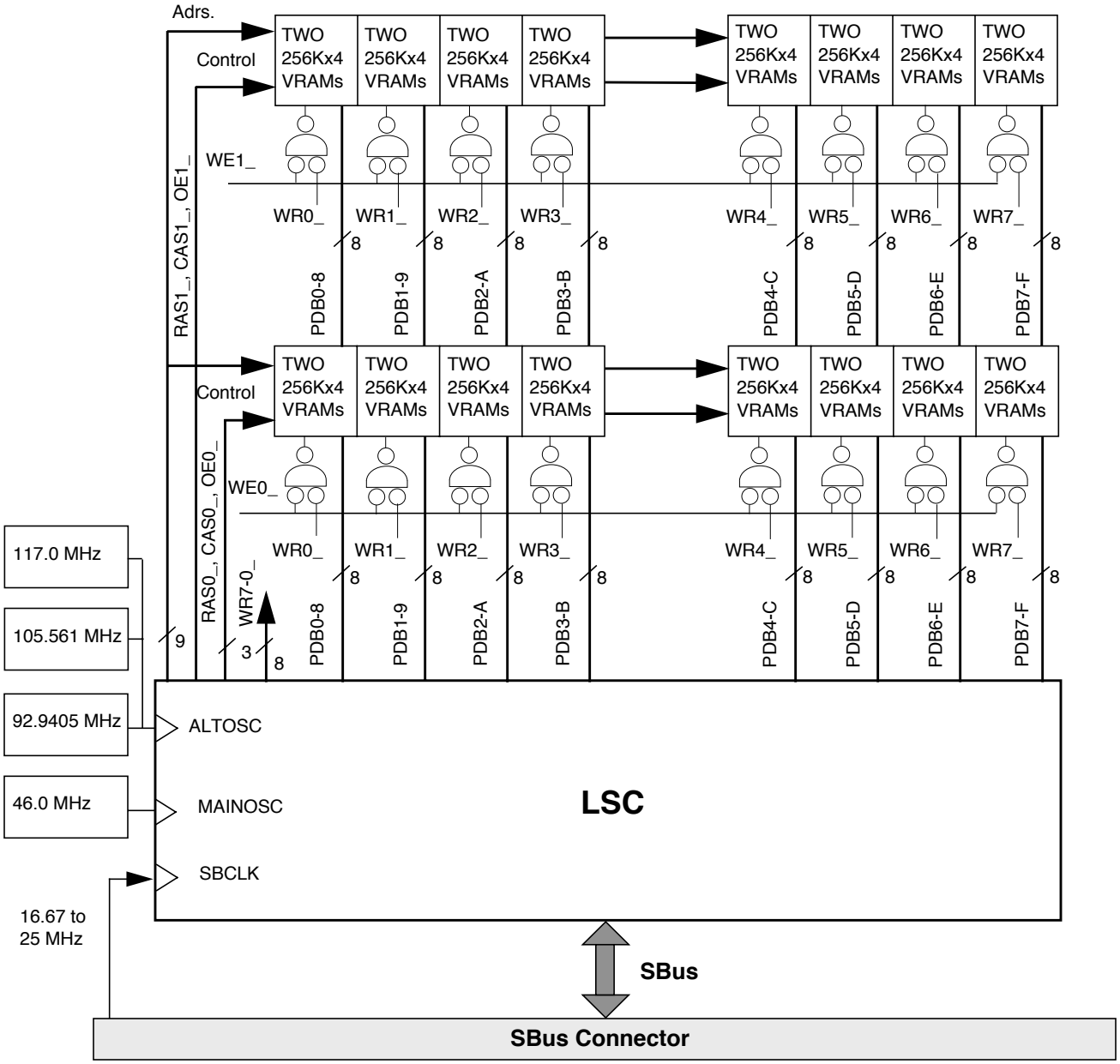


Figure 9-5 GXplus Video Memory Data Side Architecture

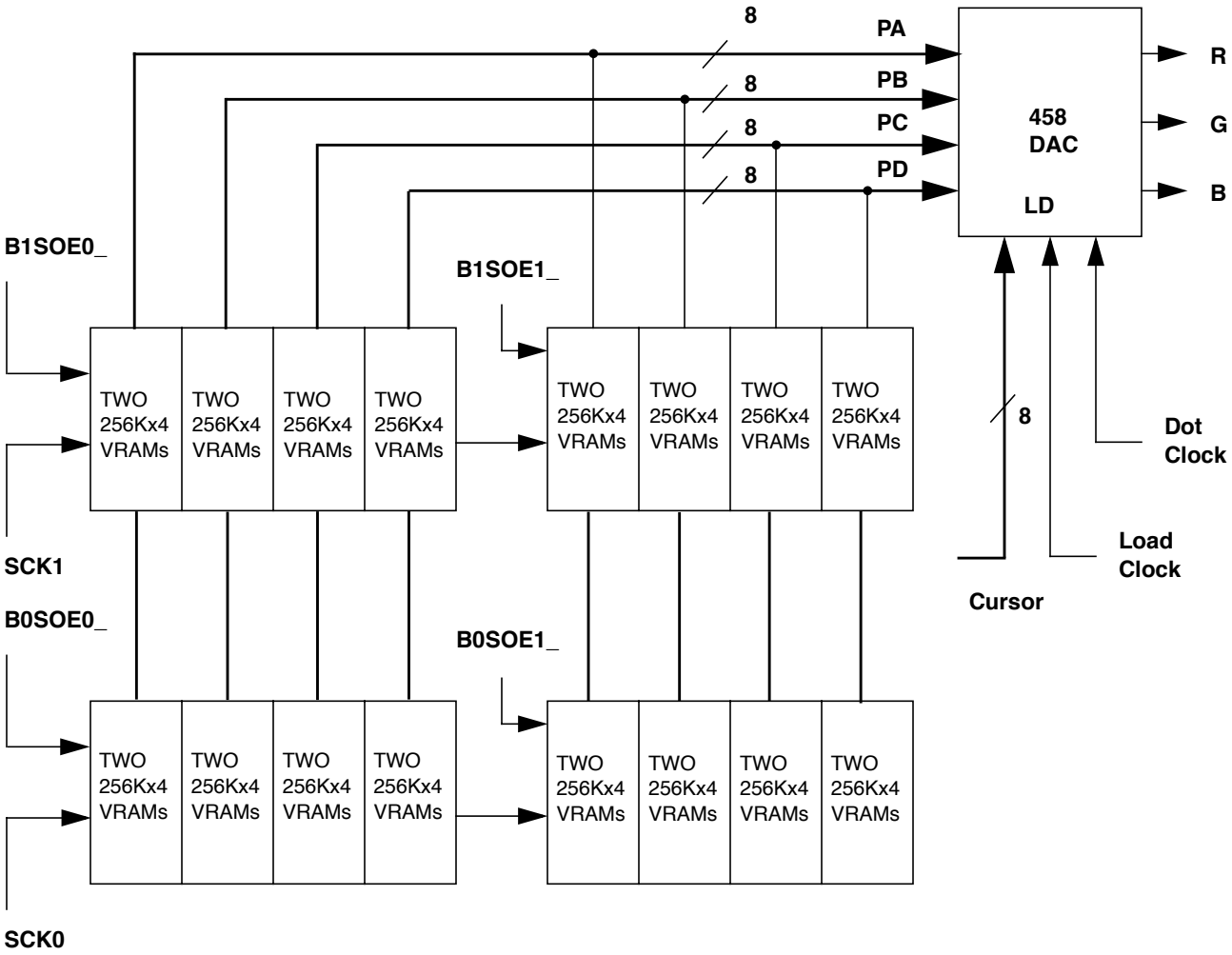


Figure 9-6 GXplus Video Memory Video Side Architecture

9.10 TurboGXplus Card

The TurboGXplus is an SBus compatible 8-bit color/greyscale graphics accelerator card. It is 100% software backward compatible with the LegoS4 and LegoP4. It can be used either with the old 66 MHz Sun color monitor or the new 76 MHz Sun color monitor. The TurboGXplus is a single-wide (146.7 mm long by 83.82 mm wide) SBus expansion card which conforms to Sun single width Sbus card specification. Refer to Chapter 1 for additional information. Figure 9-7 shows the TurboGXplus card layout.

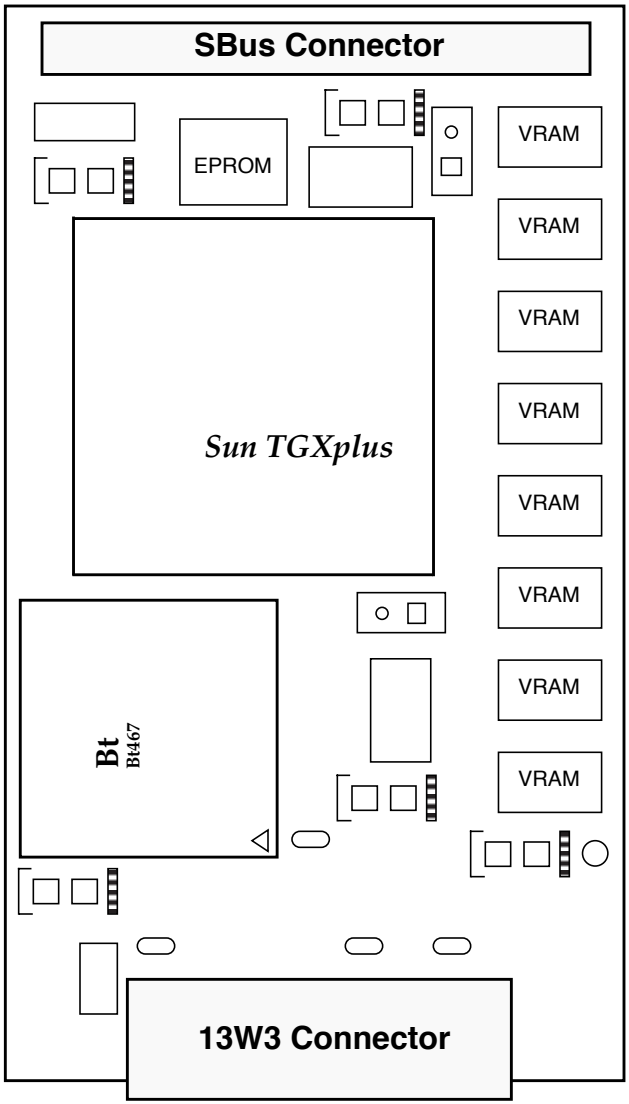


Figure 9-7 TurboGX Card Layout

9.10.1 Hardware Platform

The TurboGXplus is supported on the following Sun systems:

- SPARCstation 2
- SPARCclassic
- SPARCstation IPX
- SPARCstation 10
- SPARCstation LX
- SPARCsystem 630 MP
- SPARCsystem 670 MP
- SPARCsystem 690 MP
- SPARCcenter 1000
- SPARCcenter 2000

Refer to the TurboGX Installation Guide (800-7579) for detailed information.

9.11 TurboGXplus Specifications Summary

9.11.1 Physical Specifications

Length: 146.70 mm

Width: 83.82 mm

Weight: 5.7 Oz.

9.11.2 Electrical Specifications

9.11.2.1 Input Requirements

Current: 2.5 amps (maximum)

Power Requirements: 5 volts ± 5%

Heat dissipation: 12.5 watts

Load Condition: Running special code designed for exercising the frame buffer to the maximum power (not typical of normal applications).

9.11.3 Environmental and Reliability Specifications

Table 9-4 TurboGXplus Card Environmental and Reliability Specifications

Reliability Parameters	Specification
Temperature, operating	0 to 40 degrees C
Temperature, storage	-20 to 80 degrees C
Relative humidity, operating and storage	5 to 80% (non-condensing)
Relative humidity, non-operating	5 to 80% (non-condensing)
Altitude, operating	0 to 10,000 feet (0 to 3048 meters
Altitude, storage	0 to 40,000 feet (0 to 9144 meters)
MTTR	30 minutes or less
MTBF	165,000 hours

9.11.4 Performance

Normal operation is 50MHz clock and 1152x900@67 Hz.

Horizontal fill: 1.6 Gpixels per second

Vertical fill: 19.8 Mpixels per second

Vector and Polygon Performance: Depends on the CPU platform and software efficiency.

9.11.5 Double Buffer Support

Hardware double buffering allows two 8-bit buffers at any resolution.

9.11.6 DAC

Bt467 compatible.

9.12 Resolutions

1152x900 @66Hz

1152x900 @76Hz

1024x800 @84Hz

1024x768 @60Hz

1024x768 @70Hz

1024x768 @76Hz

1280x1024 @67 Hz

1280x1024 @76Hz

1600x1280 @76Hz

1920x1080 @72Hz

Note – The supported resolutions are subject to change.

9.13 Interface Requirements

Connector type: SBus

9.14 Agency Certification

FCC Class B

VCCI Class 2

DOC Class B

UL

CSA

TUV

9.15 Compatibility

SBus compatible.

9.15.1 Memory Devices

Uses 16 256k x 8 60 nS VRAMs. Refer to Chapter 5, “Video Memory” for additional information.

9.15.2 Component Packaging

Refer to the GXplus card specifications described earlier. The TurboGXplus card uses the same chip package.

9.15.3 Video Timing Diagrams

Refer to Chapter 5 for details.

9.15.4 Video Memory Architecture

The following figures show video memory data side and video side architecture for the TurboGX card.

Figure 9-5 shows the TurboGXplus card video memory data side architecture.

Figure 9-6 shows the video memory video side architecture of the TurboGXplus card.

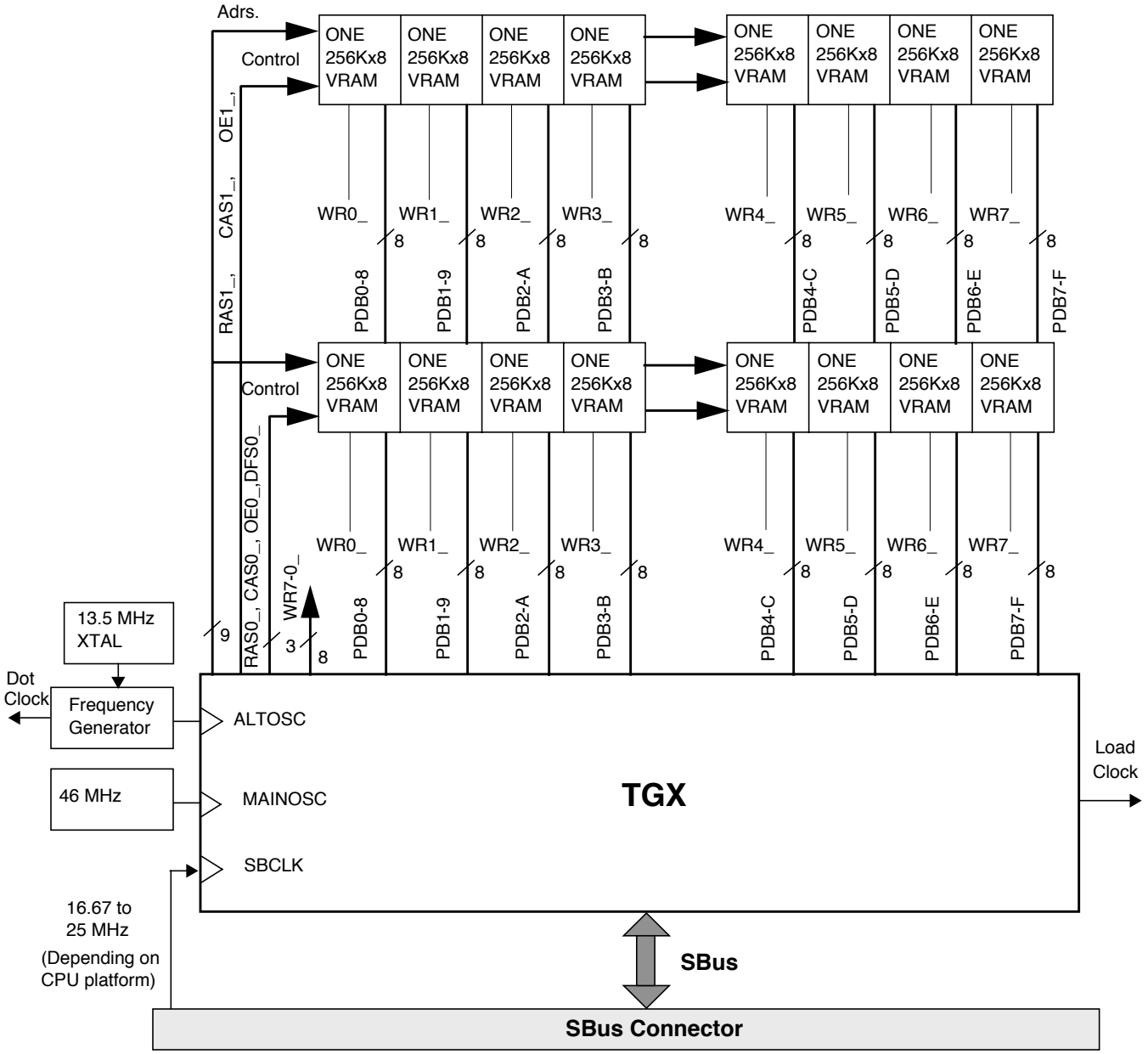


Figure 9-8 TurboGXplus Video Memory Data Side Architecture

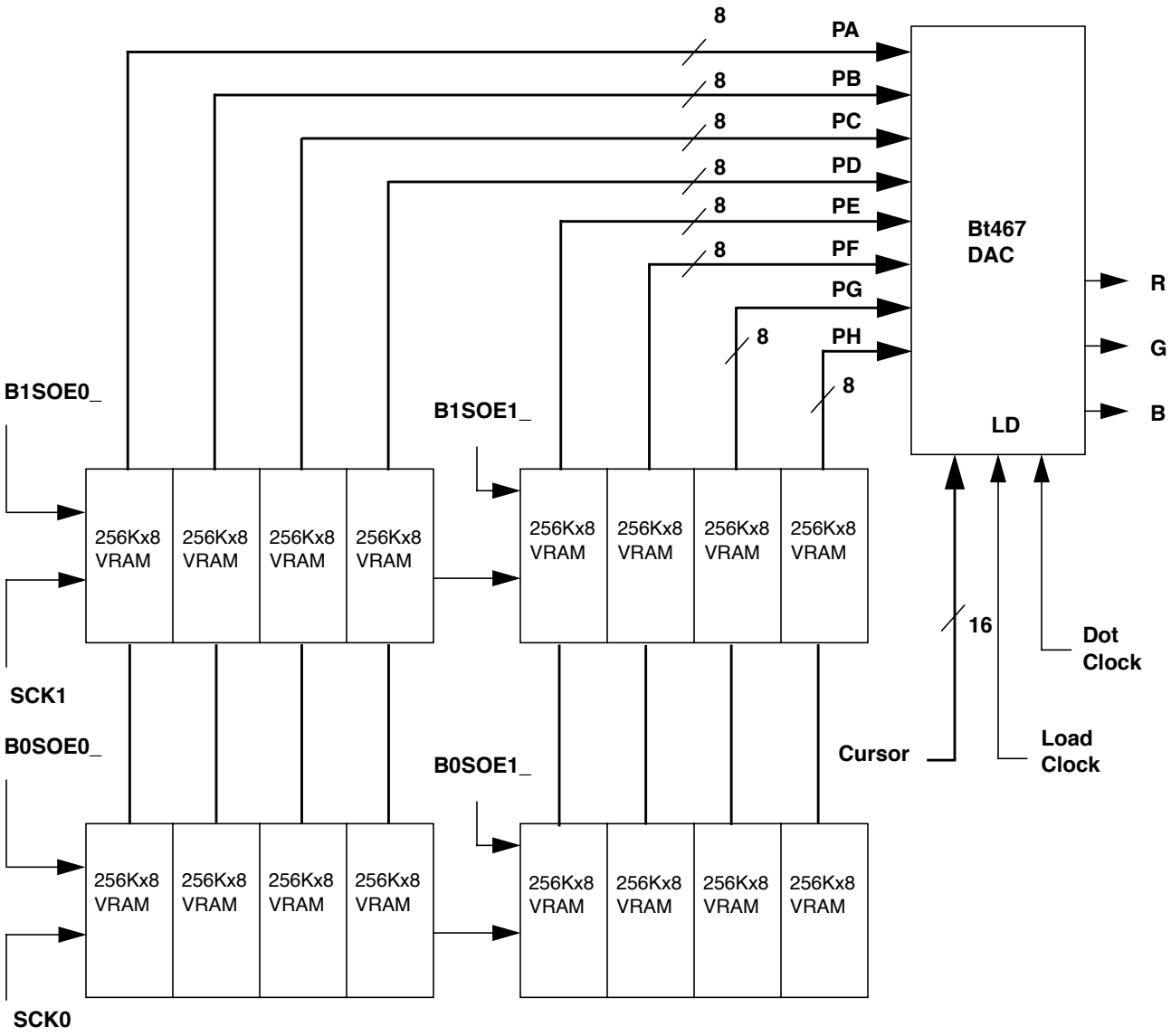


Figure 9-9 TurboGXplus Video Memory Video Side Architecture

9.16 TurboGX Specifications Summary

Refer to the TurboGXplus specification summary for detailed information.

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